Tools Tutorials
Part B

Dengxue Yan
Washington University in St. Louis

Tools mainly used in this class

Synopsys VCS	Simulation
Synopsys Design Compiler	Generate gate-level netlist
Cadence Encounter	placing and routing

Outline

Synopsys Design Compiler

Cadence Encounter

Design Compiler

- **Introduction**

  We use Synopsys Design Compiler (DC) to synthesize Verilog RTL models into a gate-level netlist where all of the gates are from the standard cell library. So Synopsys DC will synthesize the Verilog + operator into a specific arithmetic block at the gate-level. Based on various constraints it may synthesize a ripple-carry adder, a carry-look-ahead adder, or even more advanced parallel-prefix adders.

Design Compiler

- TCL File

compiledc.tcl

```
1  ##########################################################################
2  # User Defined Parameters
3  # You need to changes this parameters to fit you own design
4  ##########################################################################
5  # Give the list of your verilog files
6  # If you have single file in your design, then
7  set my_verilog_files [list Counter.v]
8
9  # If you have single file in your design
10 # set my_verilog_files [list File1.v File2.v]
11
12
13 # Set the top module of your design
14 set my_toplevel Counter
15
16 # set the clock period in ps
17 set CLK_PERIOD 50000
18
19 # setting the port of clock, this is the input Clock f
20 set CLOCK_INPUT clk
21
22
```

List all your designed verilog files here

Tell the design compiler the top module of the design
(You should not what is the top module of your design)

Specify the period of your clock input(unit: ps)
Frequency = 1/The period of clock

Specify the input of the clock of your design

Design Compiler

- **TCL File**

Setup library

```
set search_path …
set symbol_lib "vtvt_tsmc180.sdb"
```

Design Compiler

- **TCL File**

Constraint setting

`set_input_delay`
Sets input delay on pins or input ports relative to a clock signal.

`set_max_area`
Specifies the maximum area for the current design.

`set_max_delay`
Specifies a maximum delay target for selected paths in the current design.

`set_min_delay`
Specifies a minimum delay target for selected paths in the current design.

Design Compiler

- **TCL File**

  Design Compiler settings

```
check_design
check_timing
report_area
report_timing_requirements
```

Design Compiler

- TCL File

Report files define

```
redirect [format "%s%s" $my_toplevel  _design.repC] {
report_design }
redirect [format "%s%s" $my_toplevel  _area.repC]
{ report_area }
```

Design Compiler

- **TCL File**

  Other command

Look at the *Design Compiler User Guide* on blackboard for detail.

Design Compiler

- **Compile**

Compile the files by typing in the terminal:

% dc_shell-t -f <file>.tcl

In the above example, it should be:

% dc_shell-t -f compiledc.tcl

After run this command, there might be some warning but no error presented in the terminal. Otherwise you need to check your code or *tcl* file and correct them according to the related messages.

Design Compiler

- **Timing Report**

★ *<my_toplevel>_min_timing.repC*

★ *<my_toplevel>_max_timing.repC*

★ *<my_toplevel>_out_min_timing.repC*

Make sure the timing report requirements are MET. You can observe which module in the design is giving the maximum delay and optimize accordingly.

Design Compiler

```
****************************************
Report : timing
         -path full
         -delay min
         -nworst 3
         -greater_path 0.00
         -max_paths 20
Design : Counter
Version: J-2014.09-SP5
Date   : Sun Oct  2 17:39:06 2016
****************************************

Operating Conditions: nom_pvt   Library: vtvt_tsmc180
Wire Load Model Mode: top

  Startpoint: c_reg[0] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: c_reg[0] (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  c_reg[0]/ck (dp_1)                       0.00       0.00 r
  c_reg[0]/q (dp_1)                      326.98     326.98 r
  U20/op (nor2_1)                        100.13     427.12 f
  c_reg[0]/ip (dp_1)                       0.00     427.12 f
  data arrival time                                 427.12

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  c_reg[0]/ck (dp_1)                       0.00       0.00 r
  library hold time                        0.00       0.00
  data required time                                  0.00
  -----------------------------------------------------------
  data required time                                  0.00
  data arrival time                                -427.12
  -----------------------------------------------------------
  slack (MET)                                       427.12
```

Design Compiler

- **Power Report**

★ *<my_toplevel>_power.repC*

```
Global Operating Voltage = 1.8
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ps
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1mW


  Cell Internal Power  =  11.4299 uW   (77%)
  Net Switching Power  =   3.4778 uW   (23%)
                         ---------
Total Dynamic Power    =  14.9077 uW  (100%)

Cell Leakage Power     =  11.2191 nW
```

Design Compiler

- **Area Report**

★ *<my_toplevel>_area.repC*

```
****************************************
Report : area
Design : Counter
Version: J-2014.09-SP5
Date   : Sun Oct  2 17:39:06 2016
****************************************

Library(s) Used:

    vtvt_tsmc180 (File: /project/linuxlab/cadence/vendors/VTVT/vtvt_tsmc180/Synopsys_Libraries/libs/vtvt_tsmc180.db)

Number of ports:                           7
Number of nets:                           27
Number of cells:                          25
Number of combinational cells:            20
Number of sequential cells:                5
Number of macros/black boxes:              0
Number of buf/inv:                         4
Number of references:                      8

Combinational area:               836.746197
Buf/Inv area:                     111.099602
Noncombinational area:            872.612991
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 1709.359188
Total area:                 undefined
1
```

Outline

Synopsys Design Compiler

Cadence Encounter

Cadence Encounter

- **Introduction**

We use Cadence Encounter for placing and routing standard cells, but also for power routing and clock tree synthesis. The Verilog gate-level netlist generated by Synopsys DC has no physical information: it is just a netlist, so the Cadence Encounter will first try and do a rough placement of all of the gates into rows on the chip. Cadence Encounter will then do some preliminary routing, and iterate between more and more detailed placement and routing until it reaches the target cycle time (or gives up). Cadence Encounter will also route all of the power and ground rails in a grid and connect this grid to the power and ground pins of each standard cell, and Cadence Encounter will automatically generate a clock tree to distribute the clock to all sequential state elements with hopefully low skew. The automated flow for place-and-route is much more sophisticated compared to what we did in the previous tutorial.

Encounter

- View File

This is a file generated by Design Compiler.
(You need to change it according to your design)

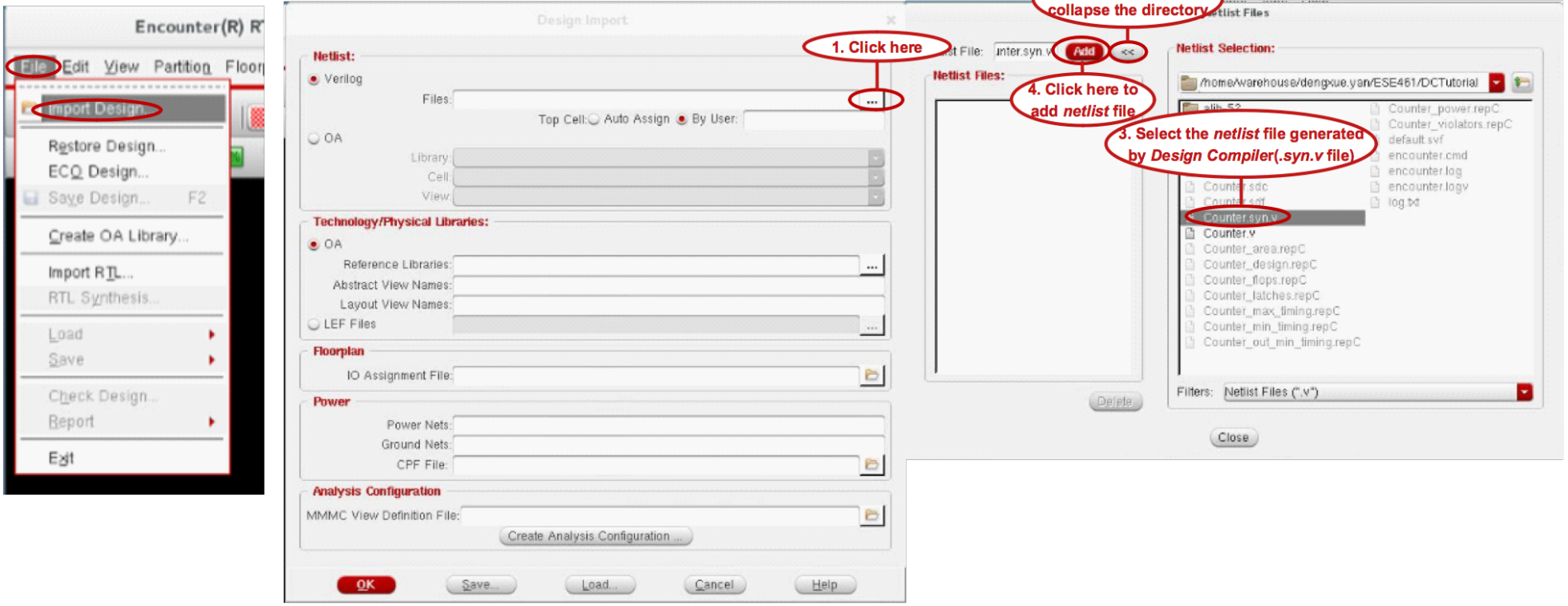
```
# Version:1.0 MMMC View Definition File
# Do Not Remove Above Line
create_library_set -name vtvt_tsmc180 -timing [/project/linuxlab/cadence/vendors/VTVT/vtvt_tsmc180/Synopsys_Libraries/libs/vtvt_tsmc180.lib]
create_constraint_mode -name constraint_rule -sdc_files {Counter.sdc}
create_delay_corner -name vtvt_tsmc180 -library_set {vtvt_tsmc180}
create_analysis_view -name constraint_rule -delay_corner vtvt_tsmc180 -constraint_mode {constraint_rule}
set_analysis_view -setup {constraint_rule} -hold {constraint_rule}
```

Encounter

- Start Encounter

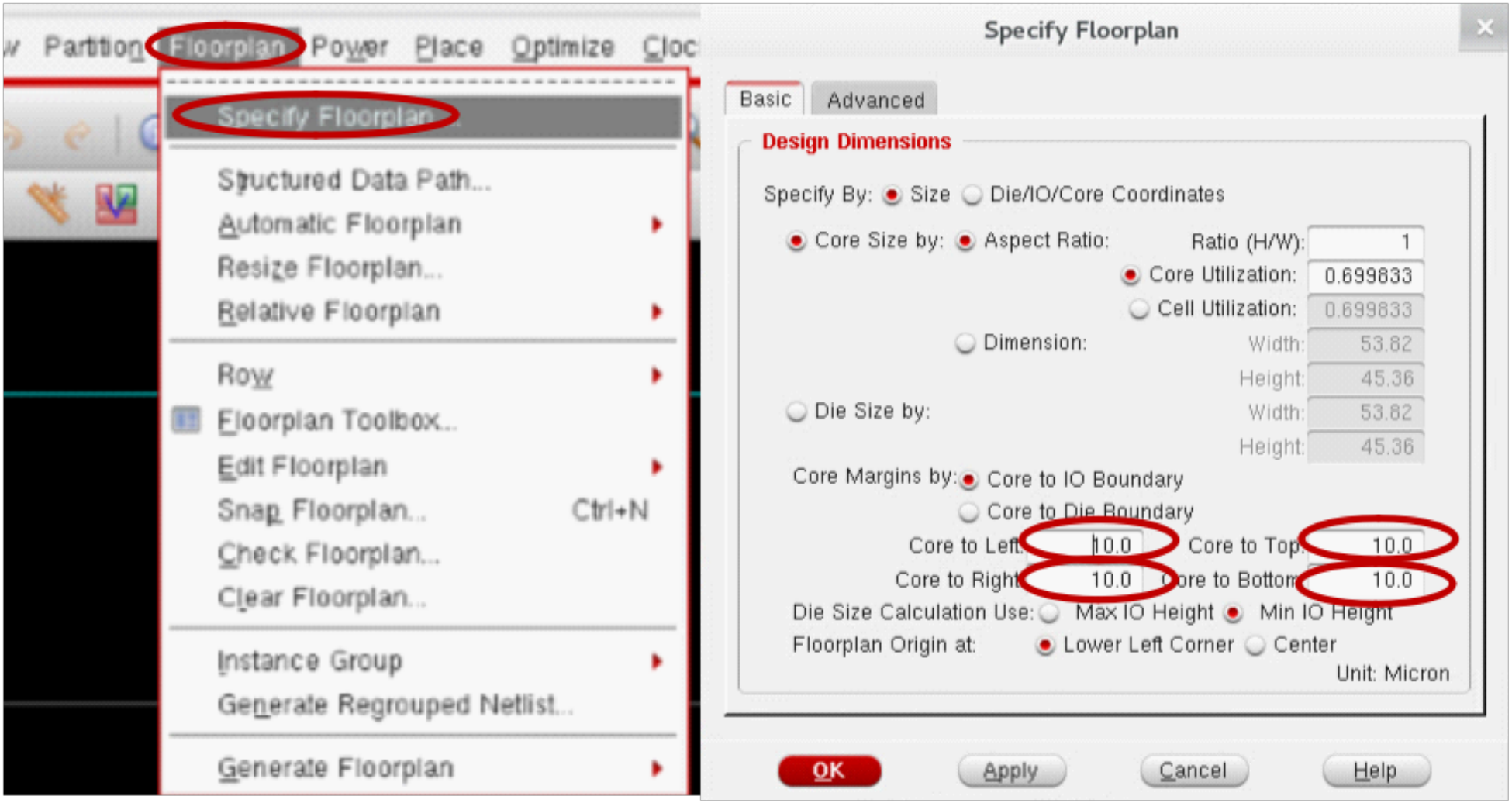
Encounter

- Import Design



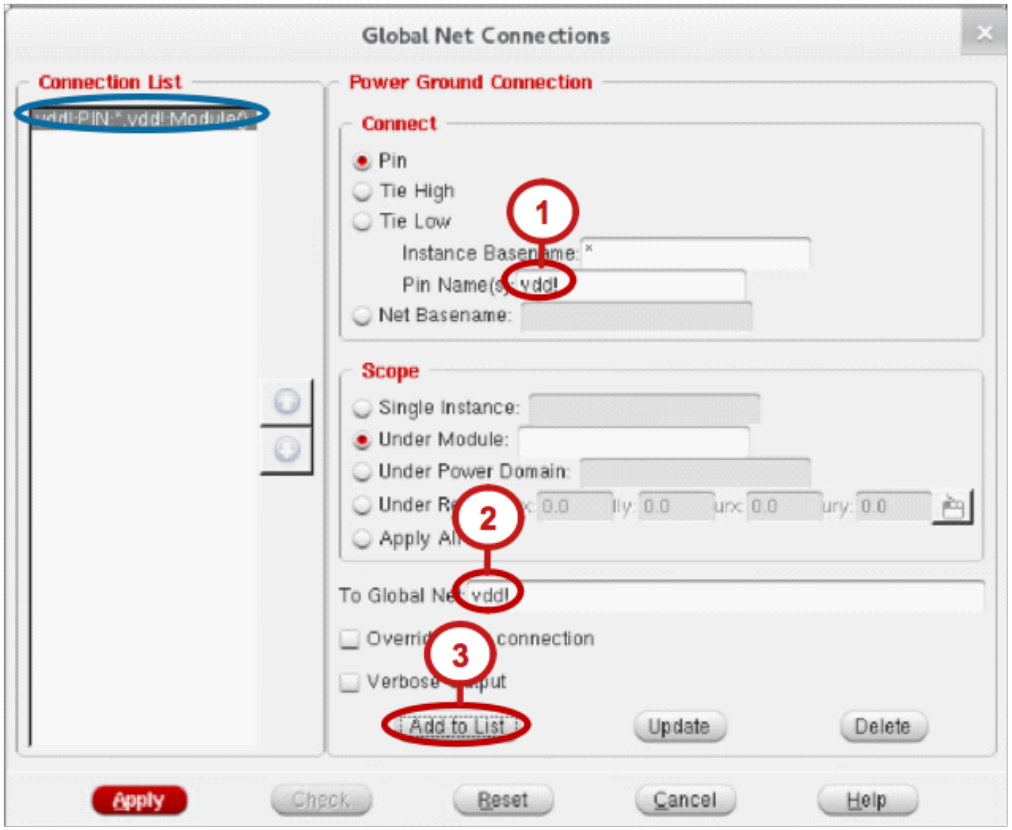
Encounter

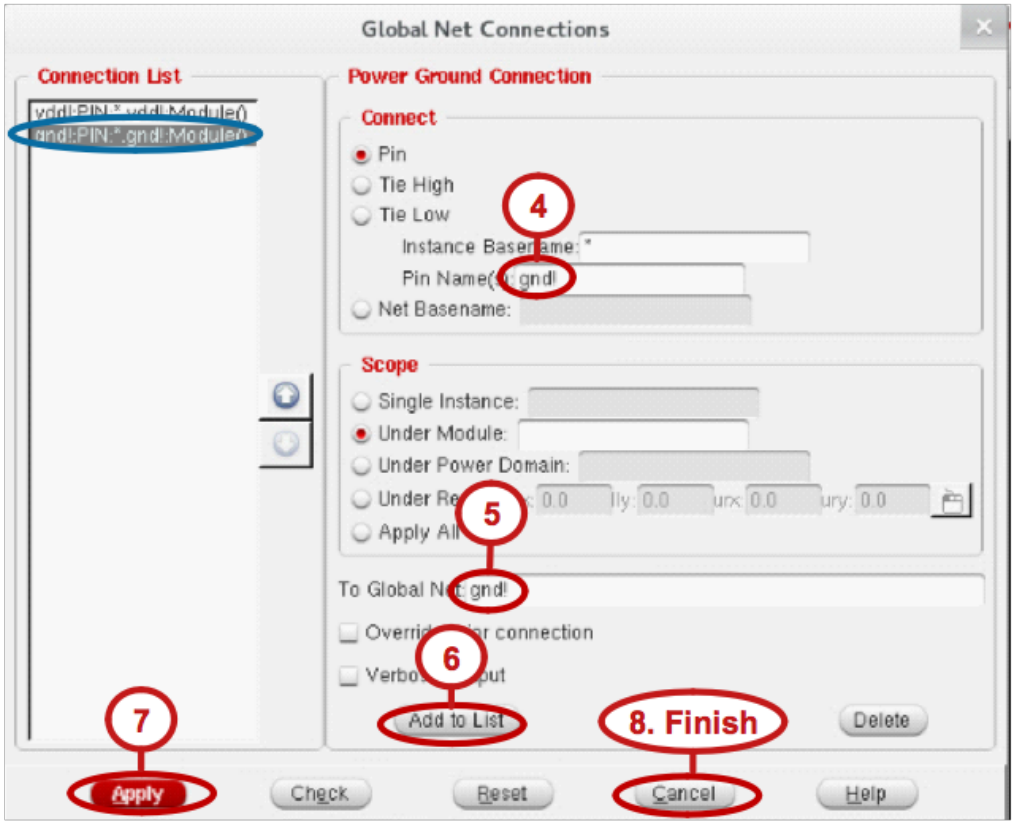
- Floor Plan



Encounter

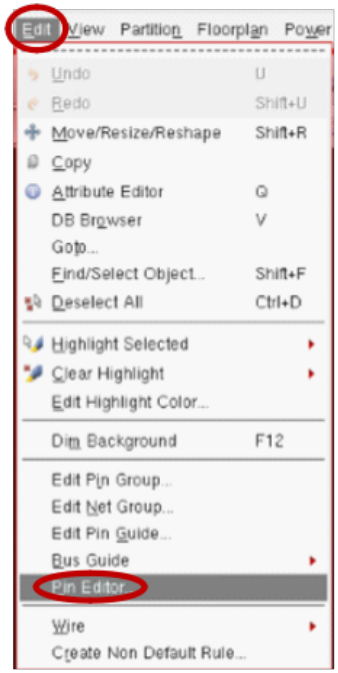
- Power Route Setting

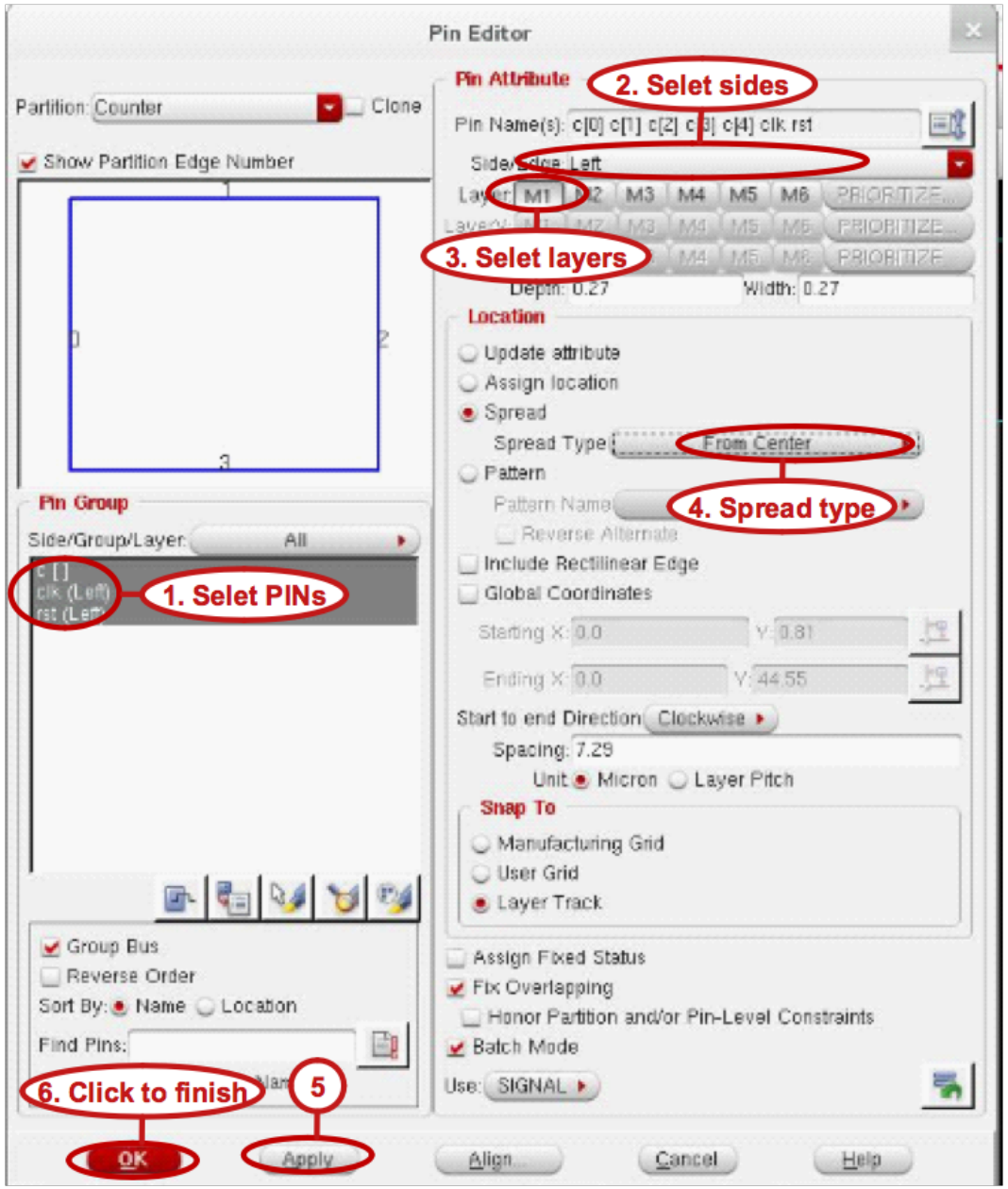




Encounter

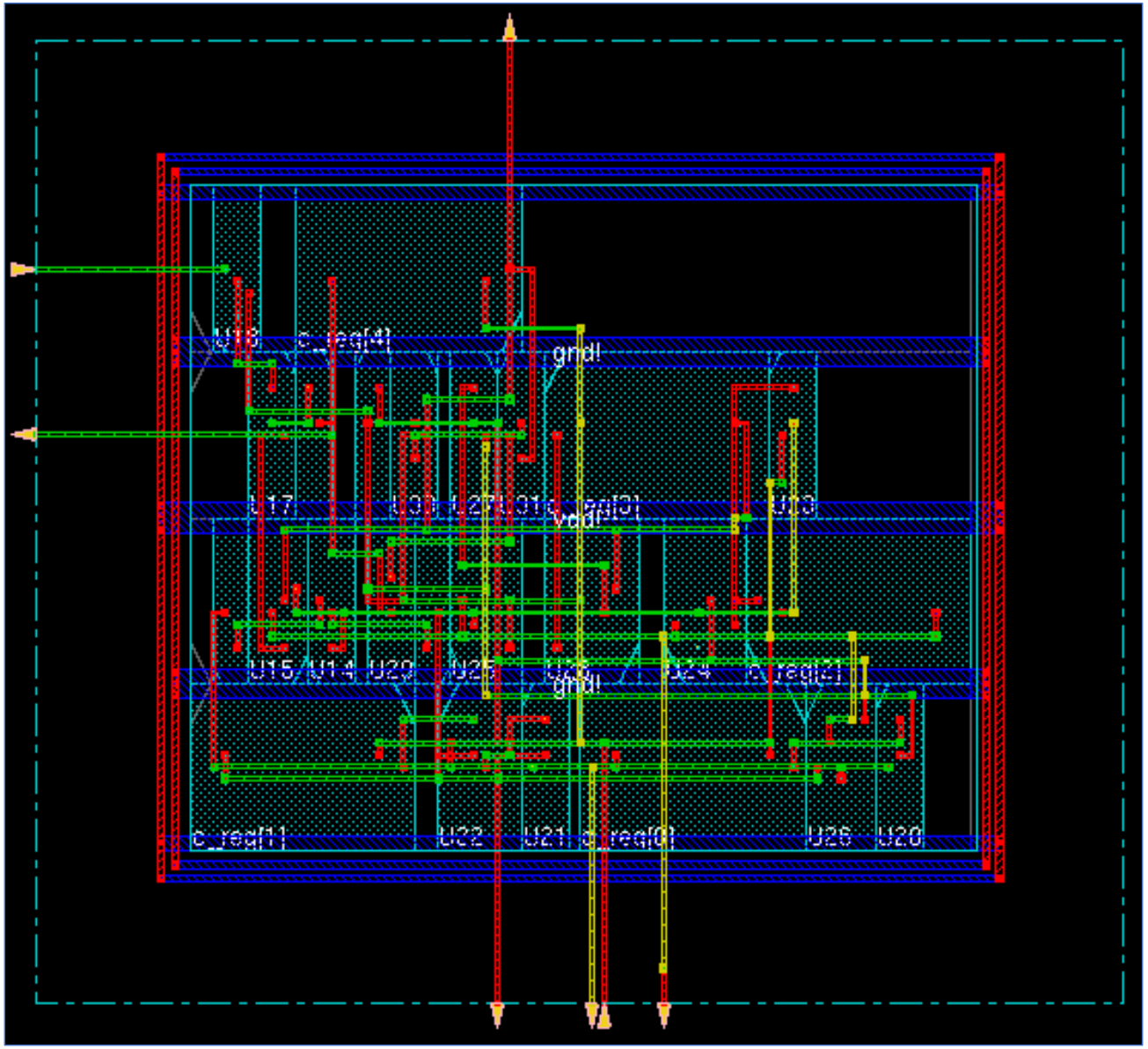
- Pins Editting





Encounter

- Place standard cell



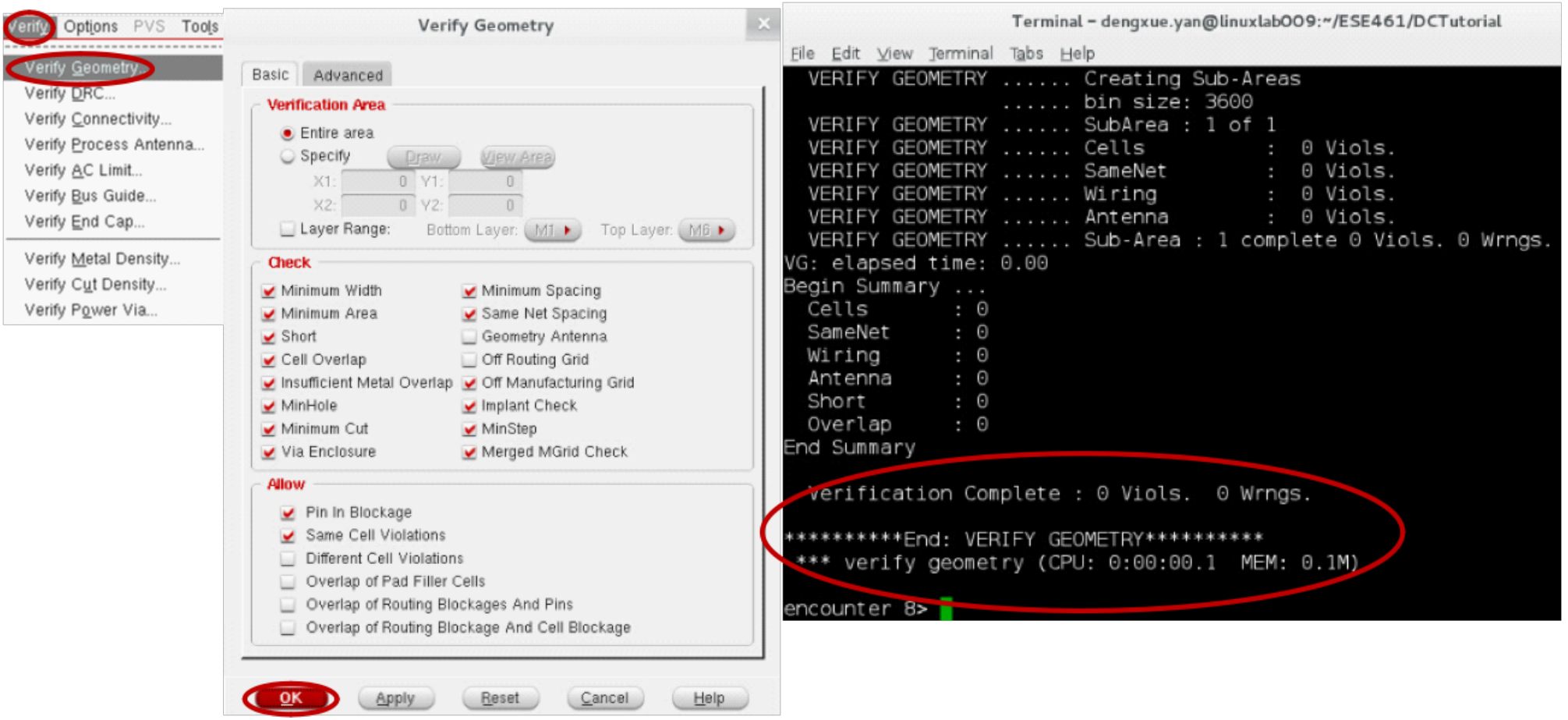
Encounter

- **Clock tree synthesis**

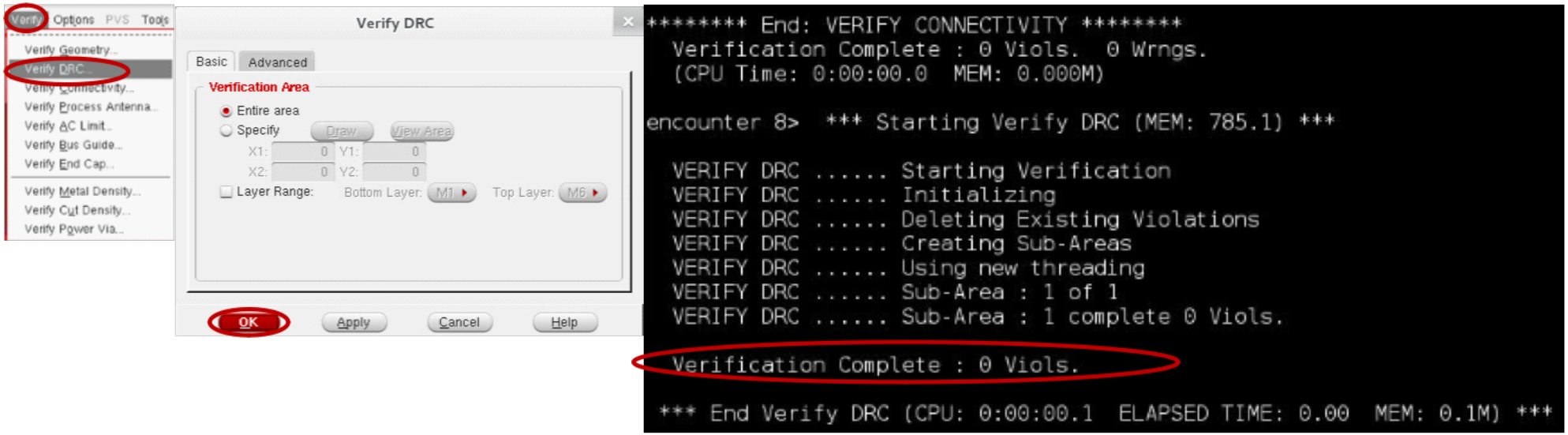
- Download *Clock.ctstch* and place it in working directory.
- Download *Clock.tcl* and place it in working directory.
- Open *Clock.tcl* using *gedit* and copy the content line by line to the *encounter terminal* and execute it.

Encounter

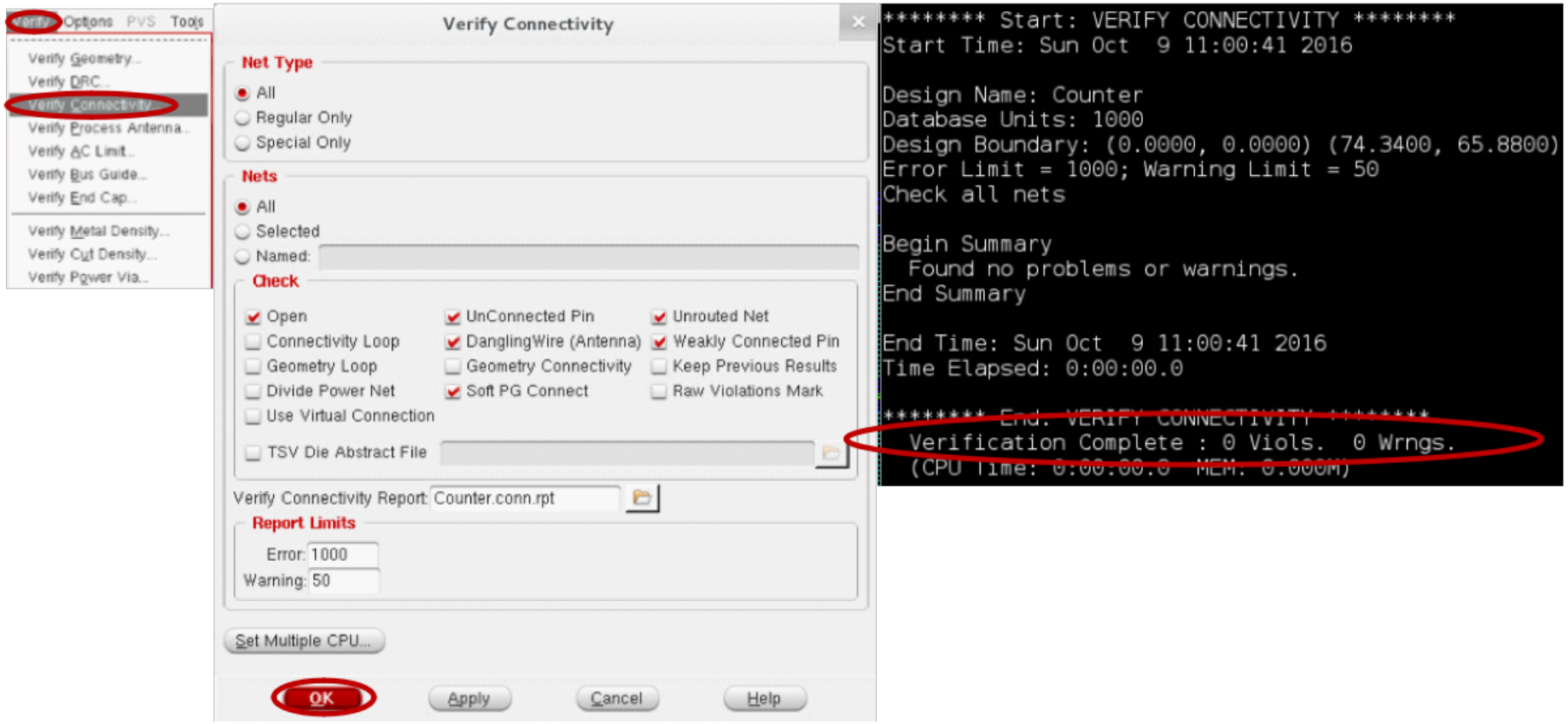
- **Verification**



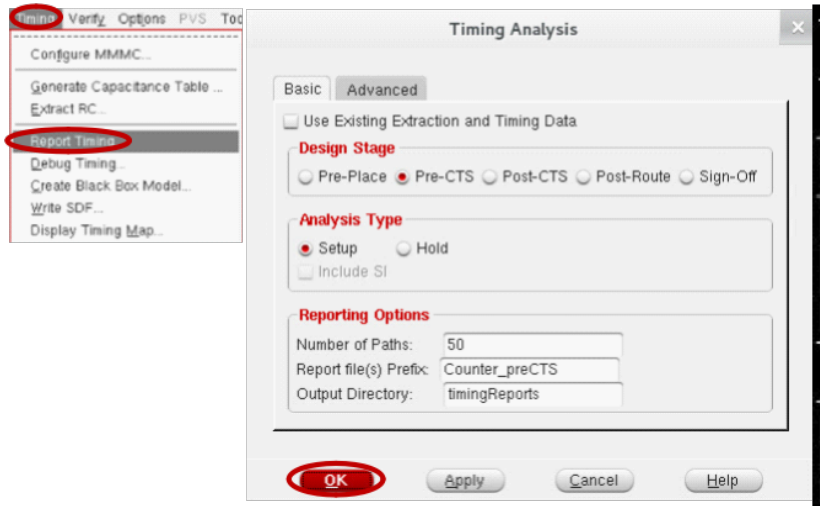
Encounter


Verify
Options
PVS
Tools
Verify Geometry...
Verify DRC...
Verify Connectivity...
Verify Process Antenna...
Verify AC Limit...
Verify Bus Guide...
Verify End Cap...
Verify Metal Density...
Verify Cut Density...
Verify Power Via...
Verify DRC
Basic
Advanced
Verification Area
Entire area
Specify
Draw
View Area
X1: 0 Y1: 0
X2: 0 Y2: 0
Layer Range:
Bottom Layer: M1
Top Layer: M6
OK
Apply
Cancel
Help
******** End: VERIFY CONNECTIVITY ********
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)
encounter 8> *** Starting Verify DRC (MEM: 785.1) ***
VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area : 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 0.1M) ***

Encounter


Verify
Options
PVS
Tools
Verify Geometry...
Verify DRC...
Verify Connectivity...
Verify Process Antenna...
Verify AC Limit...
Verify Bus Guide...
Verify End Cap...
Verify Metal Density...
Verify Cut Density...
Verify Power Via...
Verify Connectivity
Net Type
All
Regular Only
Special Only
Nets
All
Selected
Named:
Check
Open
UnConnected Pin
Unrouted Net
Connectivity Loop
DanglingWire (Antenna)
Weakly Connected Pin
Geometry Loop
Geometry Connectivity
Keep Previous Results
Divide Power Net
Soft PG Connect
Raw Violations Mark
Use Virtual Connection
TSV Die Abstract File
Verify Connectivity Report: Counter.conn.rpt
Report Limits
Error: 1000
Warning: 50
Set Multiple CPU...
OK
Apply
Cancel
Help
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Oct 9 11:00:41 2016
Design Name: Counter
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (74.3400, 65.8800)
Error Limit = 1000; Warning Limit = 50
Check all nets
Begin Summary
Found no problems or warnings.
End Summary
End Time: Sun Oct 9 11:00:41 2016
Time Elapsed: 0:00:00.0
Verification Complete : 0 Viols. 0 Wrngs.

Encounter




```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 48.248  | 48.248  | 49.017  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|         All Paths:|    5    |    5    |    5    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+-------------------+
|                |              Real             |       Total       |
|    DRVs        +------------------+------------+-------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)   |
+----------------+------------------+------------+-------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)        |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)        |
|   max_fanout   |      0 (0)       |     0      |      0 (0)        |
|   max_length   |      0 (0)       |     0      |      0 (0)        |
+----------------+------------------+------------+-------------------+

Density: 100.000%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.16 sec
Total Real time: 0.0 sec
Total Memory Usage: 683.257812 Mbytes
encounter 8>
```

Acknowledgement