



# Tools Tutorials

## Part B

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# Tools mainly used in this class



Synopsys VCS

Simulation

Synopsys Design Compiler

Generate gate-level netlist

Cadence Encounter

placing and routing

# Outline



Synopsys Design Compiler

Cadence Encounter

- **Introduction**

We use Synopsys Design Compiler (DC) to synthesize Verilog RTL models into a gate-level netlist where all of the gates are from the standard cell library. So Synopsys DC will synthesize the Verilog + operator into a specific arithmetic block at the gate-level. Based on various constraints it may synthesize a ripple-carry adder, a carry-look-ahead adder, or even more advanced parallel-prefix adders.

# Design Compiler



- **TCL File**

```
compiledc.tcl
1 #####
2 # User Defined Parameters
3 # You need to changes this parameters to fit you own design
4 #####
5 # Give the list of your verilog files
6 # If you have single file in your design, then
7 set my_verilog_files [list Counter.v]
8
9 # If you have single file in your design
10 # set my_verilog_files [list File1.v File2.v]
11
12
13 # Set the top module of your design
14 set my_toplevel Counter
15
16 # set the clock period in ps
17 set CLK_PERIOD 50000
18
19 # setting the port of clock, this is the input Clock
20 set CLOCK_INPUT clk
21
22
```

List all your designed verilog files here

Tell the design compiler the top module of the design  
(You should not what is the top module of your design)

Specify the period of your clock input(unit: ps)  
Frequency = 1/The period of clock

Specify the input of the clock of your design

# Design Compiler



- **TCL File**

## **Setup library**

```
set search_path ...  
set symbol_lib "vtvt_tsmc180.sdb"
```

# Design Compiler



- **TCL File**

## **Constraint setting**

`set_input_delay`

Sets input delay on pins or input ports relative to a clock signal.

`set_max_area`

Specifies the maximum area for the current design.

`set_max_delay`

Specifies a maximum delay target for selected paths in the current design.

`set_min_delay`

Specifies a minimum delay target for selected paths in the current design.

# Design Compiler



- **TCL File**

## **Design Compiler settings**

`check_design`

`check_timing`

`report_area`

`report_timing_requirements`



# Design Compiler



- **TCL File**

## **Report files define**

```
redirect [format "%s%s" $my_toplevel _design.repC] {  
report_design }  
redirect [format "%s%s" $my_toplevel _area.repC]  
{ report_area }
```

# Design Compiler



- **TCL File**

**Other command**

Look at the *Design Compiler User Guide* on blackboard for detail.

- **Compile**

Compile the files by typing in the terminal:

```
% dc_shell-t -f <file>.tcl
```

In the above example, it should be:

```
% dc_shell-t -f compiledc.tcl
```

After run this command, there might be some warning but no error presented in the terminal. Otherwise you need to check your code or *tcl* file and correct them according to the related messages.

- **Timing Report**

- ★ *<my\_toplevel>\_min\_timing.repC*
- ★ *<my\_toplevel>\_max\_timing.repC*
- ★ *<my\_toplevel>\_out\_min\_timing.repC*

Make sure the timing report requirements are MET. You can observe which module in the design is giving the maximum delay and optimize accordingly.

# Design Compiler



```
3 *****
4 Report : timing
5     -path full
6     -delay min
7     -nworst 3
8     -greater_path 0.00
9     -max_paths 20
10 Design : Counter
11 Version: J-2014.09-SP5
12 Date   : Sun Oct  2 17:39:06 2016
13 *****
14
15 Operating Conditions: nom_pvt   Library: vtv_tsmc180
16 Wire Load Model Mode: top
17
18 Startpoint: c_reg[0] (rising edge-triggered flip-flop clocked by clk)
19 Endpoint: c_reg[0] (rising edge-triggered flip-flop clocked by clk)
20 Path Group: clk
21 Path Type: min
22
23 Point                               Incr           Path
24 -----
25 clock clk (rise edge)                0.00           0.00
26 clock network delay (ideal)          0.00           0.00
27 c_reg[0]/ck (dp_1)                   0.00           0.00 r
28 c_reg[0]/q (dp_1)                    326.98         326.98 r
29 U20/op (nor2_1)                       100.13         427.12 f
30 c_reg[0]/ip (dp_1)                   0.00           427.12 f
31 data arrival time                     427.12
32
33 clock clk (rise edge)                0.00           0.00
34 clock network delay (ideal)          0.00           0.00
35 c_reg[0]/ck (dp_1)                   0.00           0.00 r
36 library hold time                     0.00           0.00
37 data required time                    0.00
38 -----
39 data required time                    0.00
40 data arrival time                     -427.12
41 -----
42 slack (MET)                           427.12
43
```

# Design Compiler



- Power Report

★ `<my_toplevel>_power.repC`

```
20 Global Operating Voltage = 1.8
21 Power-specific unit information :
22     Voltage Units = 1V
23     Capacitance Units = 1.000000ff
24     Time Units = lps
25     Dynamic Power Units = 1mW      (derived from V,C,T units)
26     Leakage Power Units = 1mW
27
28
29     Cell Internal Power   = 11.4299 uW   (77%)
30     Net Switching Power  =  3.4778 uW   (23%)
31     | | | | | | | | | | | | | | | |
32 Total Dynamic Power      = 14.9077 uW   (100%)
33
34 Cell Leakage Power       = 11.2191 nW
35
```

# Design Compiler



- Area Report

★ *<my\_toplevel>\_area.repC*

```
1 |
2 | *****
3 | Report : area
4 | Design : Counter
5 | Version: J-2014.09-SP5
6 | Date   : Sun Oct  2 17:39:06 2016
7 | *****
8 |
9 | Library(s) Used:
10 |
11 |     vtv_tsmc180 (File: /project/linuxlab/cadence/vendors/VTVT/vtv_tsmc180/Synopsys_Libraries/libs/vtv_tsmc180.db)
12 |
13 | Number of ports:                7
14 | Number of nets:                 27
15 | Number of cells:                25
16 | Number of combinational cells:  20
17 | Number of sequential cells:     5
18 | Number of macros/black boxes:   0
19 | Number of buf/inv:              4
20 | Number of references:           8
21 |
22 | Combinational area:              836.746197
23 | Buf/Inv area:                   111.099602
24 | Noncombinational area:          872.612991
25 | Macro/Black Box area:           0.000000
26 | Net Interconnect area:          undefined (No wire load specified)
27 |
28 | Total cell area:                 1709.359188
29 | Total area:                      undefined
30 | 1
31 |
```

# Outline



Synopsys Design Compiler

**Cadence Encounter**



# Cadence Encounter



## • Introduction

We use Cadence Encounter for placing and routing standard cells, but also for power routing and clock tree synthesis. The Verilog gate-level netlist generated by Synopsys DC has no physical information: it is just a netlist, so the Cadence Encounter will first try and do a rough placement of all of the gates into rows on the chip. Cadence Encounter will then do some preliminary routing, and iterate between more and more detailed placement and routing until it reaches the target cycle time (or gives up). Cadence Encounter will also route all of the power and ground rails in a grid and connect this grid to the power and ground pins of each standard cell, and Cadence Encounter will automatically generate a clock tree to distribute the clock to all sequential state elements with hopefully low skew. The automated flow for place-and-route is much more sophisticated compared to what we did in the previous tutorial.

# Encounter



- View File

```
1 # Version:1.0 MSGC View Definition File
2 # Do Not Remove Above Line
3 create_library_set -name vtv_tsmc180 -timing [/project/linuxlab/cadence/vendors/VTVT/vtv_tsmc180/Synopsys_Libraries/libs/vtv_tsmc180.lib]
4 create_constraint_mode -name constraint_rule -sdc_files {Counter.sdc}
5 create_delay_corner -name vtv_tsmc180 -library_set {vtv_tsmc180}
6 create_analysis_view -name constraint_rule -delay_corner vtv_tsmc180 -constraint_mode {constraint_rule}
7 set_analysis_view -setup {constraint_rule} -hold {constraint_rule}
8
```

This is a file generated by Design Compiler.  
(You need to change it according to your design)

# Encounter

- Start Encounter



```
Terminal - dengxue.yan@linuxlab009:~/E5E461/DCTutorial
File Edit View Terminal Tabs Help
[dengxue.yan@linuxlab809 ~]# cd E5E461/
[dengxue.yan@linuxlab809 E5E461]# cd DCTutorial/
[dengxue.yan@linuxlab809 DCTutorial]# module add e5e461
[dengxue.yan@linuxlab809 DCTutorial]# encounter
WARNING: HOST <linuxlab009.seas.wustl.edu> DOES NOT APPEAR TO BE A CADENCE SUPPORTED LINUX CONFIGURATION.
For More Info, Please Run '<cdsroot>/tools.lnx85/bin/checkSysConf' <productId>.

Checking out Encounter license ...
edsxl DENIED: "Encounter Digital Impl Sys XL"
edsl DENIED: "Encounter_Digital_Impl_Sys_L"
encblk DENIED: "Encounter_Block"
fegxl DENIED: "First Encounter_CXL"
fexl DENIED: "FE_GPS"
nru DENIED: "NanoRoute Ultra"
vdxl DENIED: "Virtuoso Digital Implem XL"
vdl CHECKED OUT: "Virtuoso_Digital_Implem"
Virtuoso_Digital_Implem 14.2 license checkout succeeded.
Maximum number of instance allowed (1 x 50000).
*****
* Copyright (c) Cadence Design Systems, Inc. 1996 - 2014. *
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@(#)CDS: IQRC/TQRC 14.1.6-s260 (64bit) Mon Mar 2 11:26:49 PST 2015 (Linux 2.6.18-194.el5)
@(#)CDS: OA 22.50-p011 Tue Nov 11 03:24:55 2014
@(#)CDS: SGN 10.10-p124 (19-Aug-2014) (64 bit executable)
@(#)CDS: RCDB 11.5
--- Starting "Encounter v14.23-s044_1" on Sat Oct 8 15:22:12 2016 (mem=89.1M) ---
--- Running on linuxlab009.seas.wustl.edu (x86_64 w/Linux 3.10.0-327.22.2.el7.x86_64) ---
This version was compiled on Fri Mar 20 11:30:09 PDT 2015.
Set DBUPerIGU to 1000.
Set net toggle Scale Factor to 1.00
Set Shrink Factor to 1.00000

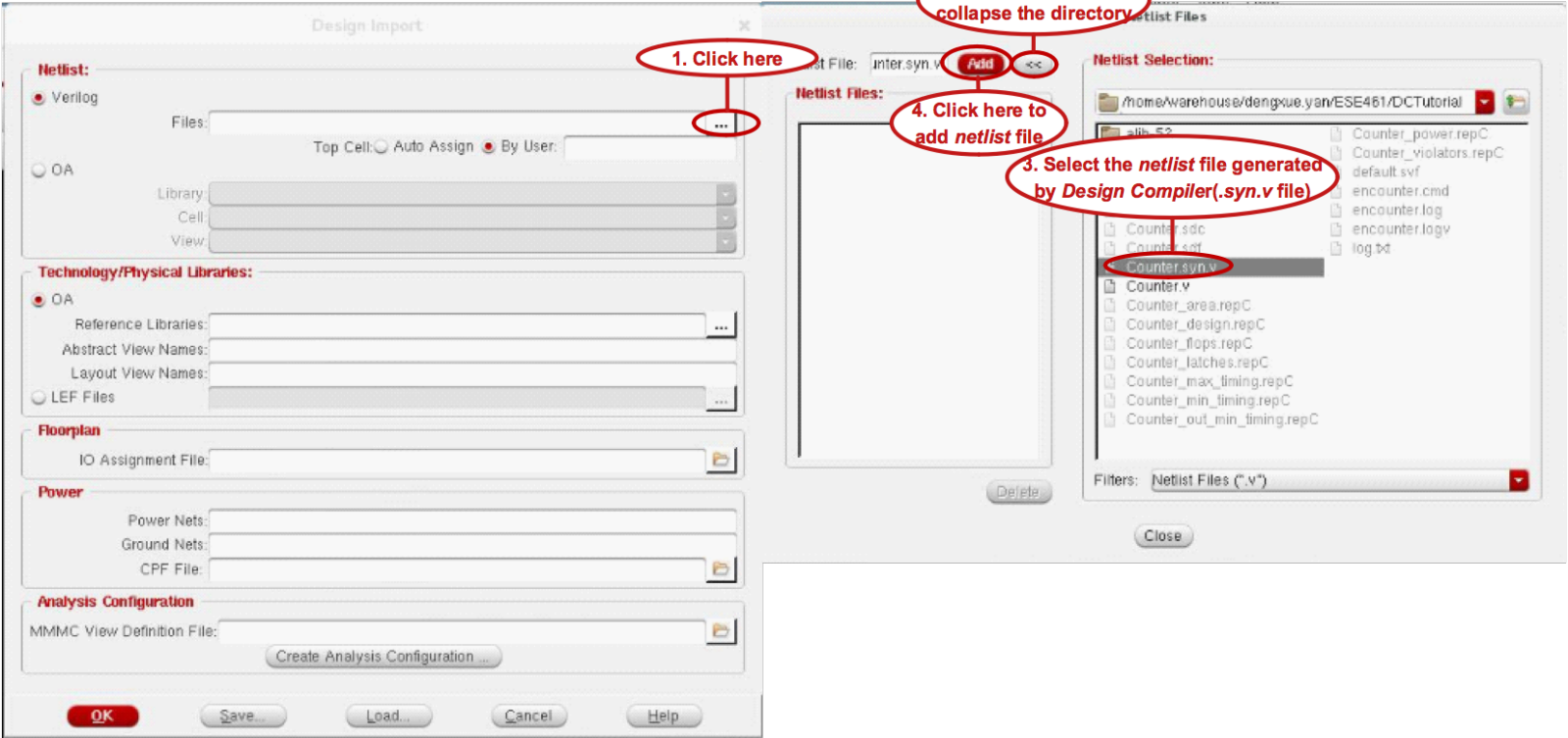
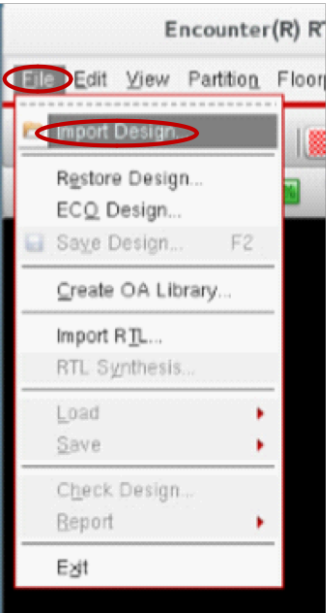
**INFO: MMIO transition support version v31-84

encounter 1> █
```

# Encounter



- Import Design



# Encounter

- Floor Plan



The image shows a screenshot of the Encounter software interface. On the left, the 'Floorplan' menu is open, with 'Specify Floorplan' highlighted. On the right, the 'Specify Floorplan' dialog box is shown, with the 'Basic' tab selected. The 'Design Dimensions' section is visible, showing options for 'Specify By' (Size, Die/IO/Core Coordinates), 'Core Size by' (Aspect Ratio, Core Utilization, Cell Utilization, Dimension), and 'Die Size by' (Core Margins by: Core to IO Boundary, Core to Die Boundary). The 'Core Margins by' section has four input fields: 'Core to Left' (10.0), 'Core to Top' (10.0), 'Core to Right' (10.0), and 'Core to Bottom' (10.0). The 'Die Size Calculation Use' section has 'Max IO Height' and 'Min IO Height' options, with 'Min IO Height' selected. The 'Floorplan Origin at' section has 'Lower Left Corner' and 'Center' options, with 'Lower Left Corner' selected. The 'Unit: Micron' is indicated at the bottom right. The 'OK', 'Apply', 'Cancel', and 'Help' buttons are at the bottom.

**Specify Floorplan**

Basic | Advanced

**Design Dimensions**

Specify By:  Size  Die/IO/Core Coordinates

Core Size by:  Aspect Ratio: Ratio (H/W): 1

Core Utilization: 0.699833

Cell Utilization: 0.699833

Dimension: Width: 53.82

Height: 45.36

Die Size by: Width: 53.82

Height: 45.36

Core Margins by:  Core to IO Boundary

Core to Die Boundary

Core to Left: 10.0 Core to Top: 10.0

Core to Right: 10.0 Core to Bottom: 10.0

Die Size Calculation Use:  Max IO Height  Min IO Height

Floorplan Origin at:  Lower Left Corner  Center

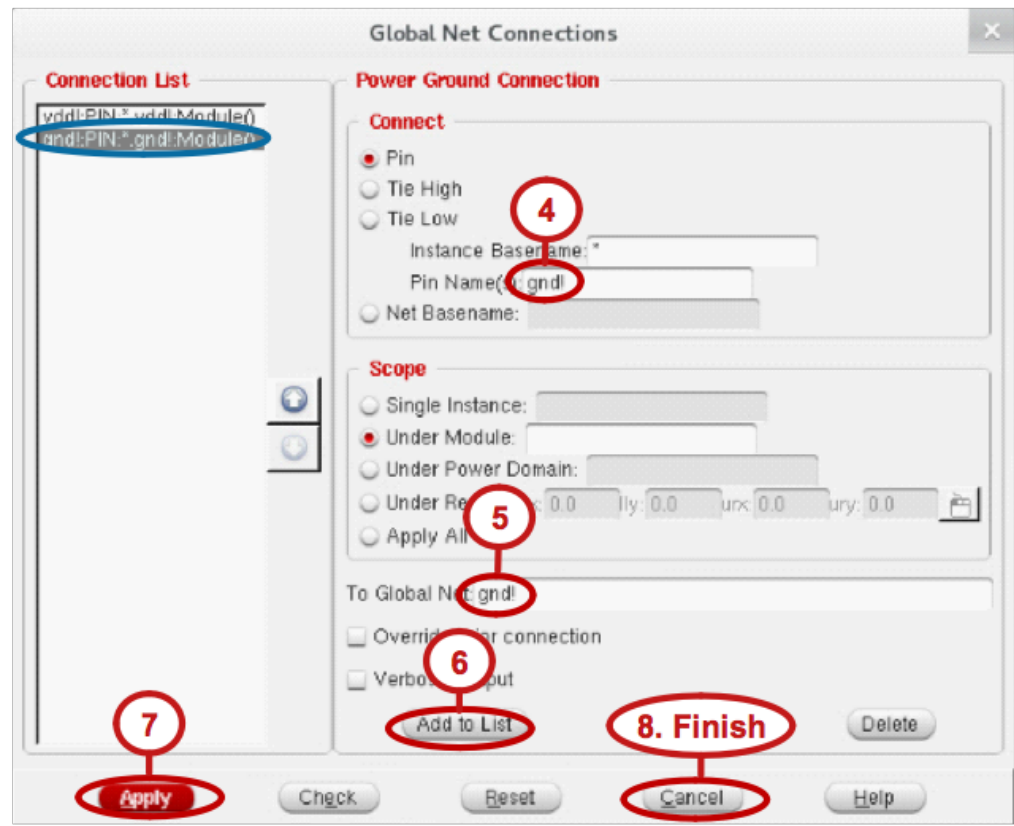
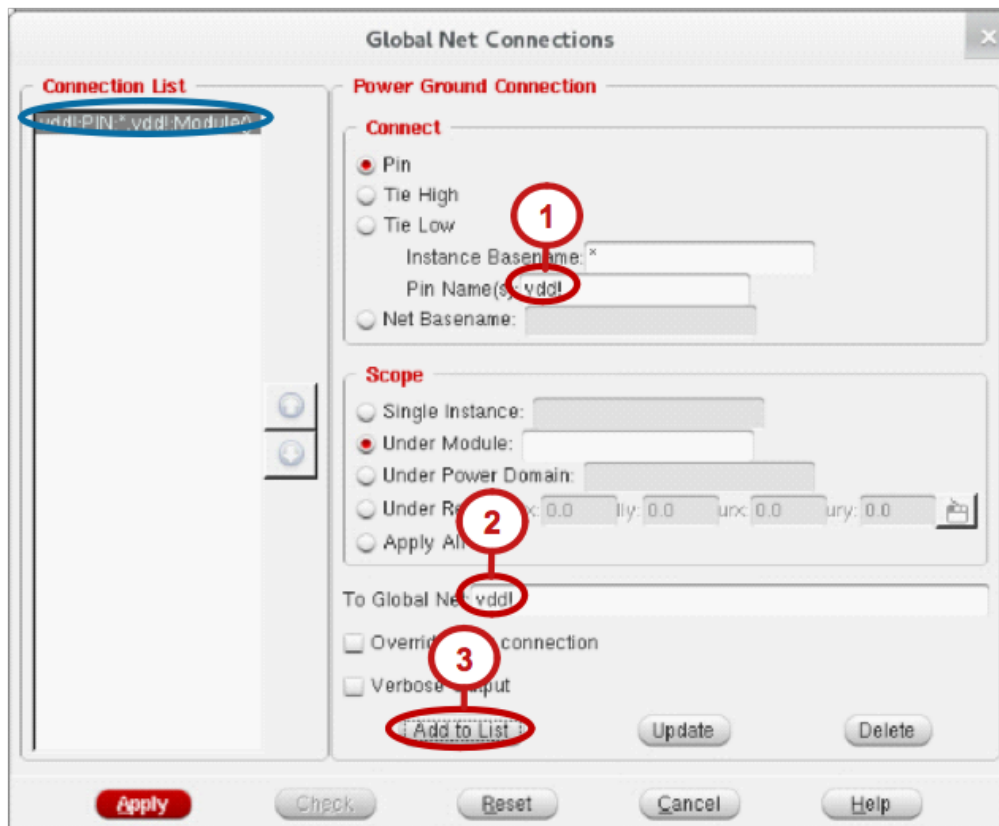
Unit: Micron

OK Apply Cancel Help

# Encounter

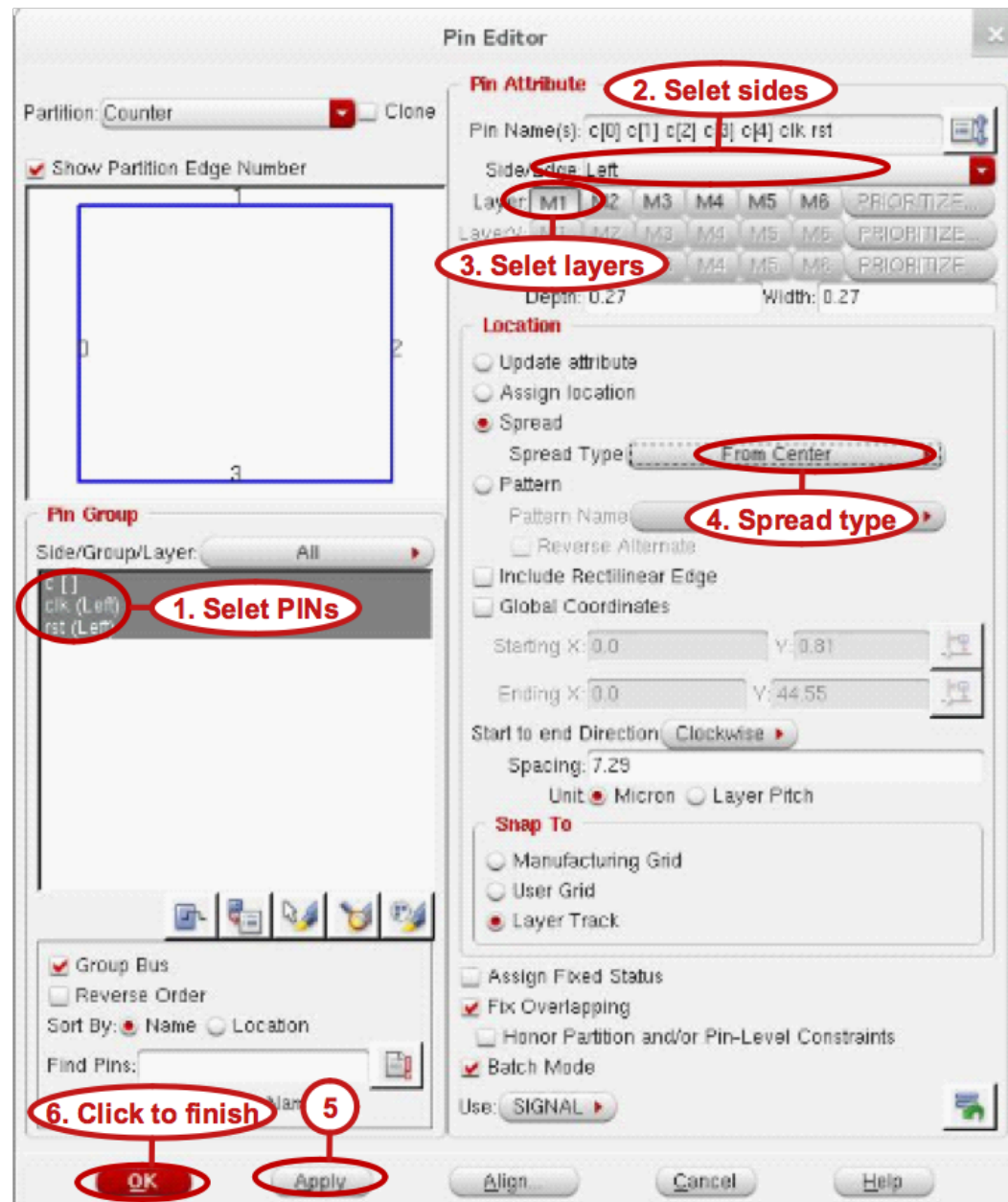


- Power Route Setting



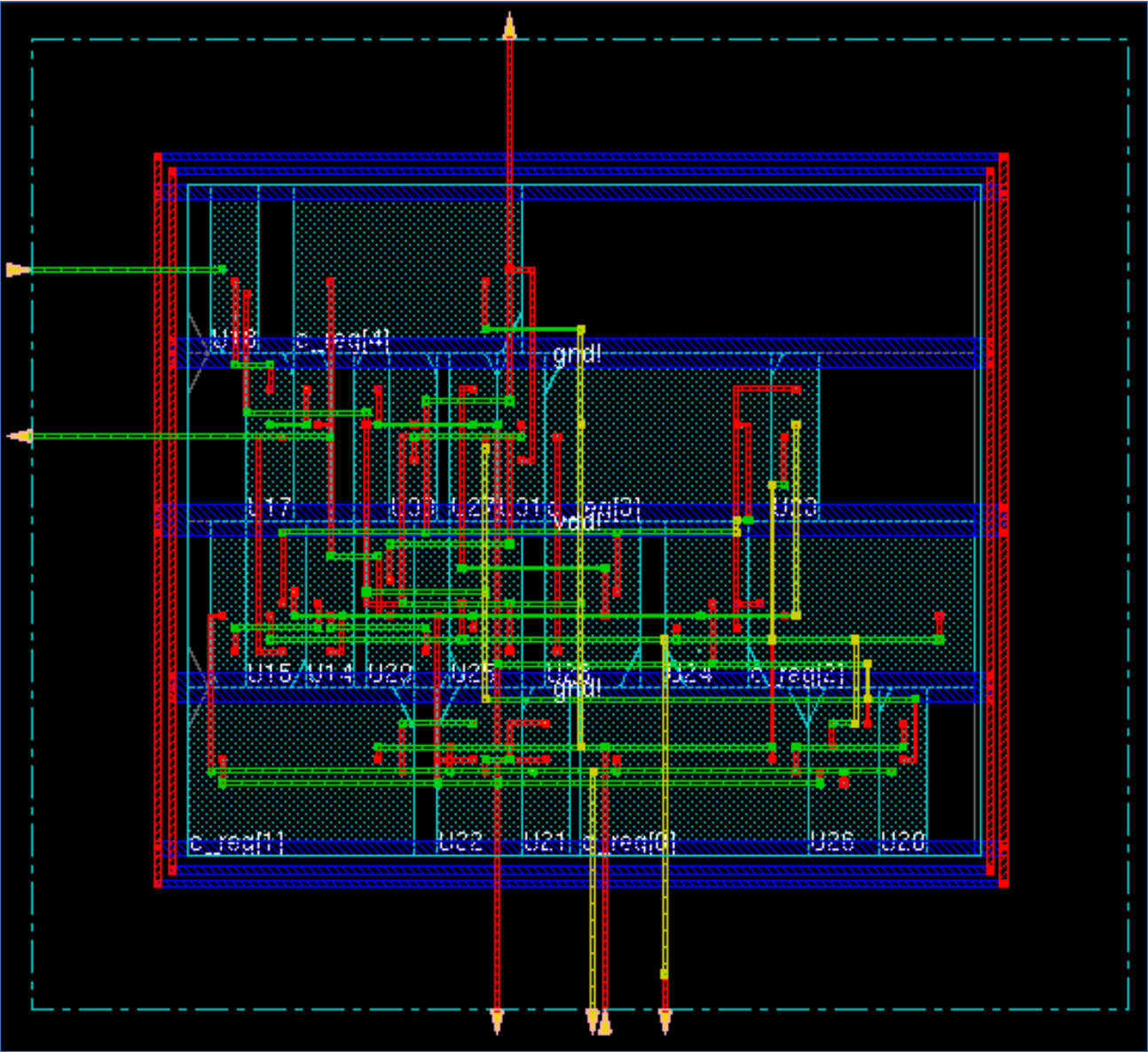
# Encounter

- Pins Editing



# Encounter

- Place standard cell





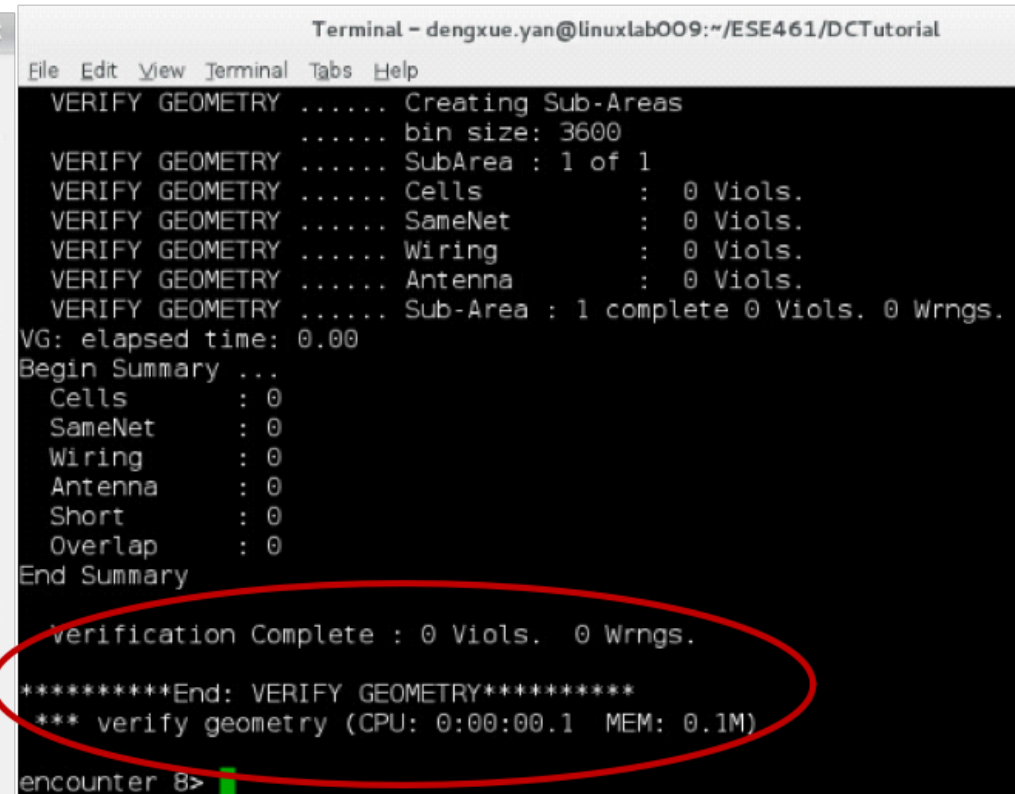
- **Clock tree synthesis**

- ✦ Download [Clock.ctstch](#) and place it in working directory.
- ✦ Download [Clock.tcl](#) and place it in working directory.
- ✦ Open *Clock.tcl* using *gedit* and copy the content line by line to the *encounter terminal* and execute it.

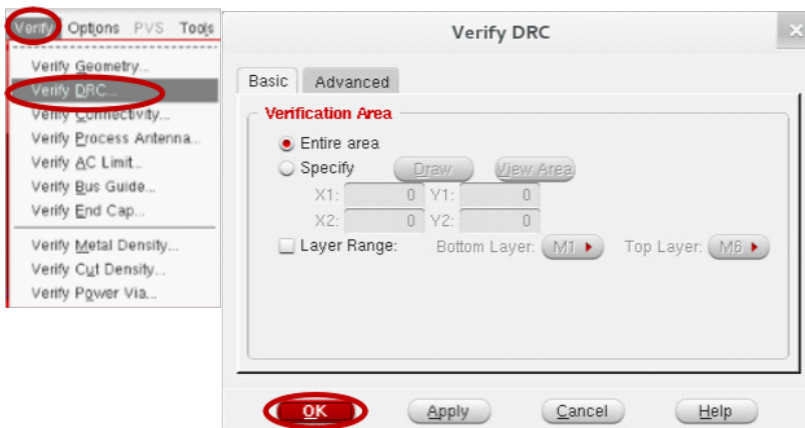
# Encounter



- Verification



# Encounter



```
***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

encounter 8> *** Starting Verify DRC (MEM: 785.1) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area : 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1 ELAPSED TIME: 0.00 MEM: 0.1M) ***
```

# Encounter



The screenshot shows the 'Verify Connectivity' dialog box in the Encounter software. The 'Verify' menu is open, with 'Verify Connectivity' selected. The dialog box has the following settings:

- Net Type:** All (selected)
- Nets:** All (selected)
- Check:** Open, UnConnected Pin, Unrouted Net, Connectivity Loop, Dangling Wire (Antenna), Weakly Connected Pin, Geometry Loop, Geometry Connectivity, Keep Previous Results, Divide Power Net, Soft PG Connect, Raw Violations Mark, Use Virtual Connection, TSV Die Abstract File (empty)
- Report Limits:** Error: 1000, Warning: 50

The terminal output on the right shows the following text:

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Sun Oct 9 11:00:41 2016

Design Name: Counter
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (74.3400, 65.8800)
Error Limit = 1000; Warning Limit = 50
Check all nets

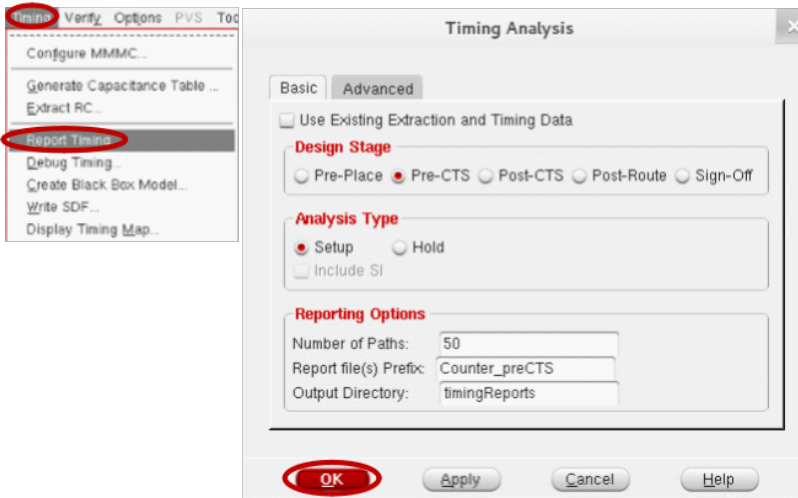
Begin Summary
Found no problems or warnings.
End Summary

End Time: Sun Oct 9 11:00:41 2016
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU time: 0:00:00.0 MEM: 0.000M)
```

Red circles highlight the 'Verify' menu, the 'Verify Connectivity' option, the 'OK' button, and the 'Verification Complete' line in the terminal output.

# Encounter



```

timeDesign Summary
-----
+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+
| WNS (ns):  | 48.248 | 48.248 | 49.017 |
| TNS (ns):  | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 5 | 5 | 5 |
+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total |
|-----|-----|-----|
| Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0 (0) |
| max_tran | 0 (0) | 0 (0) |
| max_fanout | 0 (0) | 0 (0) |
| max_length | 0 (0) | 0 (0) |
+-----+-----+-----+

Density: 100.000%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.16 sec
Total Real time: 0.0 sec
Total Memory Usage: 683.257812 Mbytes
encounter 8> █
    
```



# Acknowledgement