ESE 566A: Modern System-on-Chip Design

Homework 3

Due: Feb 6, 2:30 pm

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1. (Inverter Chain)

In this problem you will choose the number of stages and the sizing for the inverter chain shown in Fig.1 a. You should assume that the input capacitance of the first inverter is C_u, $\gamma = 1$, and t_{inv} is the unit delay of an inverter as defined in lecture (i.e., $t_p = t_{inv(\gamma+f)}$).

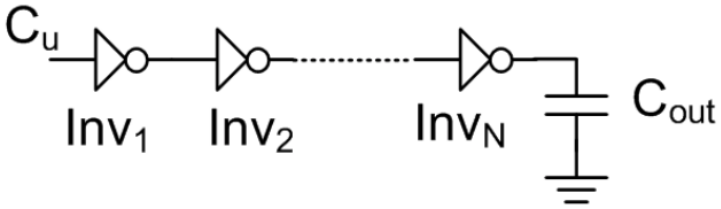


Fig.1 a

a) Given that $C_{out} = 624*C_u$, what is the optimal number of stages to use for this inverter chain? (Note that you don't need to worry about the logical polarity of the signal.)

b) Using your answer to part a), what is the optimal delay of the inverter chain?

c) Now let's look at the the chain of just two inverters shown in Fig.1 b, with given C_{out}, C_u, and $R_2 = k*R_{inv1}$ (where R_{inv1} is the on resistance of the first inverter). What C_2 (input cap of the second inverter) gives the minimum delay?

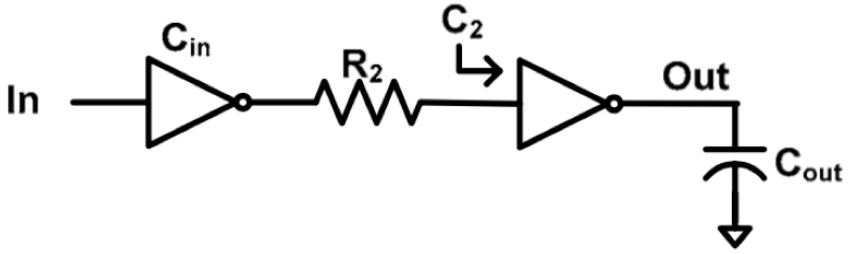


Fig.1 b

2. (Power and Delay)

Throughout this problem, you should ignore all the capacitors associated with the transistors – i.e., you can assume that the only capacitors are those explicitly shown in the circuit. Also, you can ignore shoot-through current, and you can assume that the leakage current is equal to $\frac{W}{L} I_O e^{\left(\frac{-V_T}{1.5\times 25mV}\right)}$, where $I_{O,NMOS} = 4\mu A$ and $I_{O,PMOS} = 2\mu A$.

Now consider the 2-input NAND gate shown below:

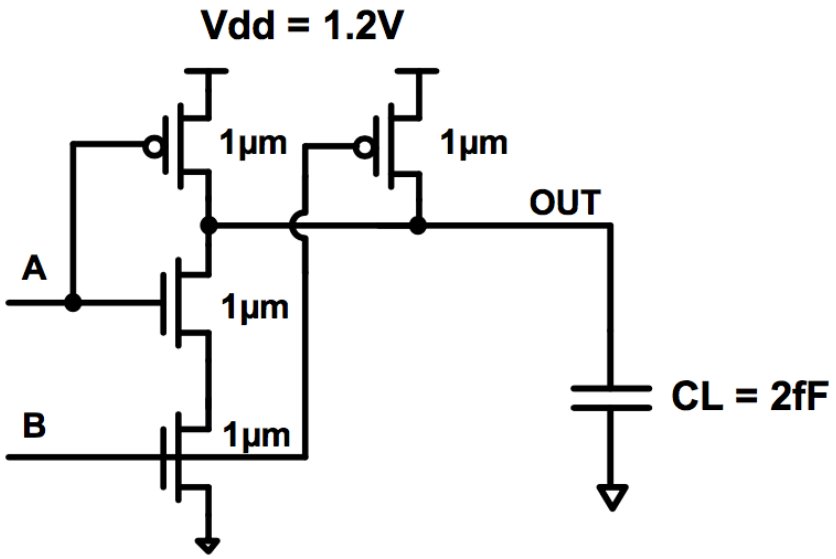


Fig.2 a

a) Calculate the leakage current for all 4 possible states of the 2 inputs A and B.

b) Assuming that the inputs A and B are driven with the waveforms shown below in Fig.2 b that these waveforms repeat every 3ns, calculate the average dynamic power drawn from the supply.

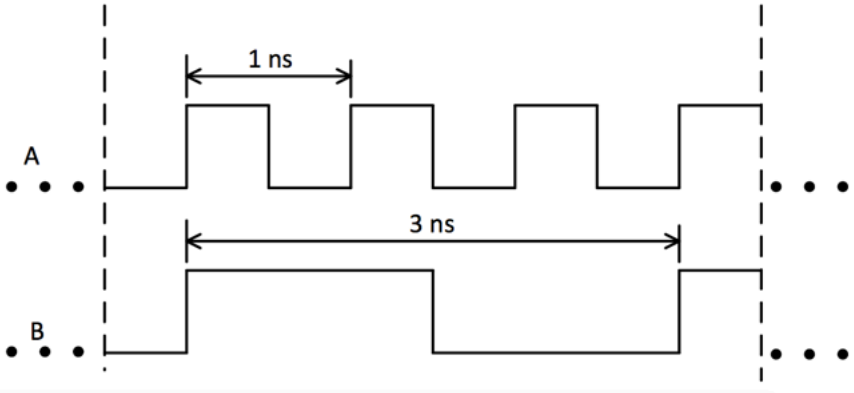


Fig.2 b

c) Calculate the average total power drawn from the supply with the same inputs which is shown in part b).

3. (Wires, Delay, and Ratioed Logic)

For this problem, you should assume that all of the transistors are minimum channel length (L=0.1µm) and have the following characteristics: $C_G = C_D = 2fF/\mu m^2$ and $R_{sqn} = R_{sqp}/2 = 10k\Omega/\square$. For the wires, you should assume that $C_{wpp} = 0.05fF/\mu m$, $C_{wfringe} = 0.075fF/\mu m/edge$, and $R_{sqw} = 0.1\Omega/\square$.

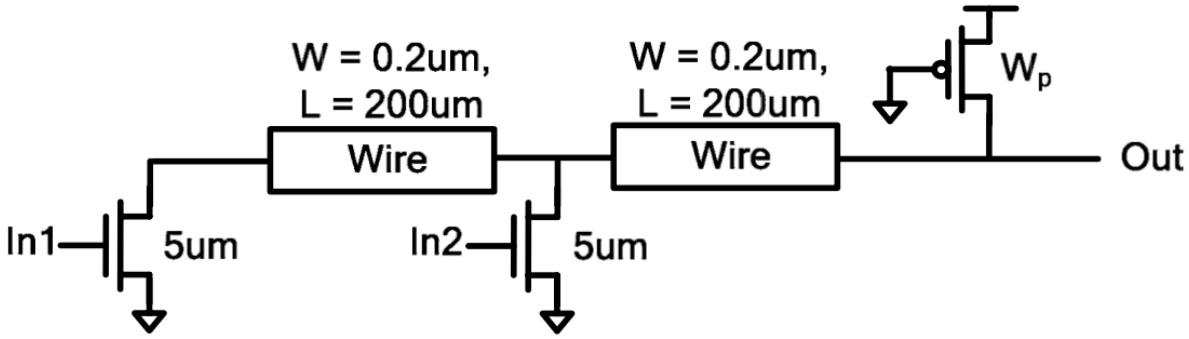


Fig.3

a) For the circuit shown above, size the PMOS pull-up transistor (i.e., choose W_p) so that the pull-up resistance of the gate is equal to 4 times the worst-case pull-down resistance.

b) Assuming that you found that W_p = 1.25um in order for the pull-up resistance to be 4 times larger than the worst-case pull-down resistance (as shown above – note that this may or may not be the right answer to part a)), what is the worst-case ramp delay of the circuit?

4. (Sequential Elements)
In this problem we will be examining the latch shown below.

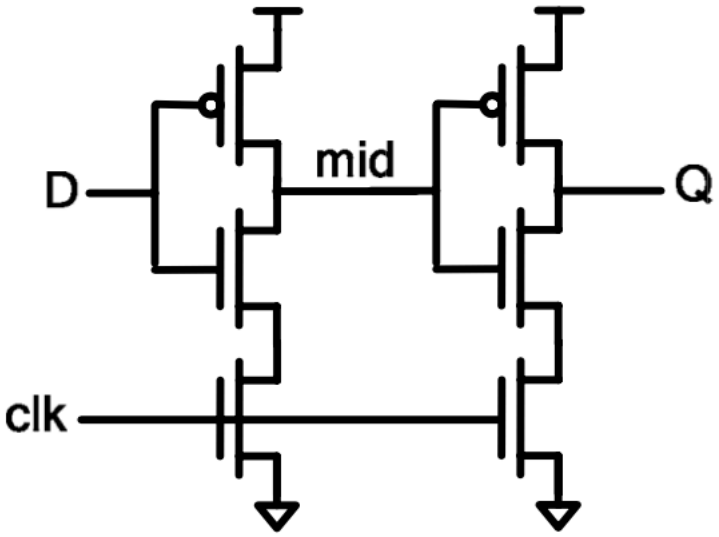


Fig.4 a

Assuming the latch is ideal (i.e., has no delay, zero setup/hold time, etc.), fill in the waveforms for mid and Q given the clock and data inputs shown below.

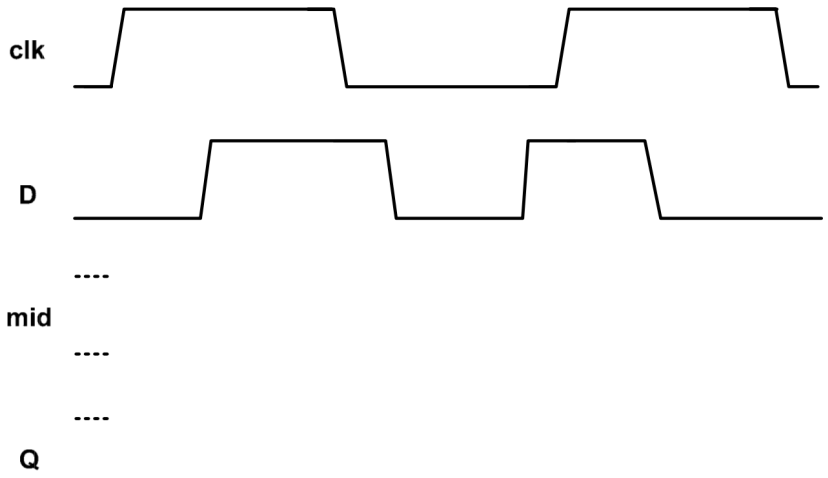


Fig.4 b

5. (Logic Styles and Logic Effort (LE))

For this problem, you can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10k\Omega/\square$, $R_{sqp} = 20k\Omega/\square$, and that the transistors are quadratic (i.e., long-channel).

a) Given the sizing shown below, what value of W would you use in order to make the worst-case LE of the C input equal to half the LE of the A and B inputs (i.e., LEC = 1⁄2LEA)? What would be the LE of the C input in this case?

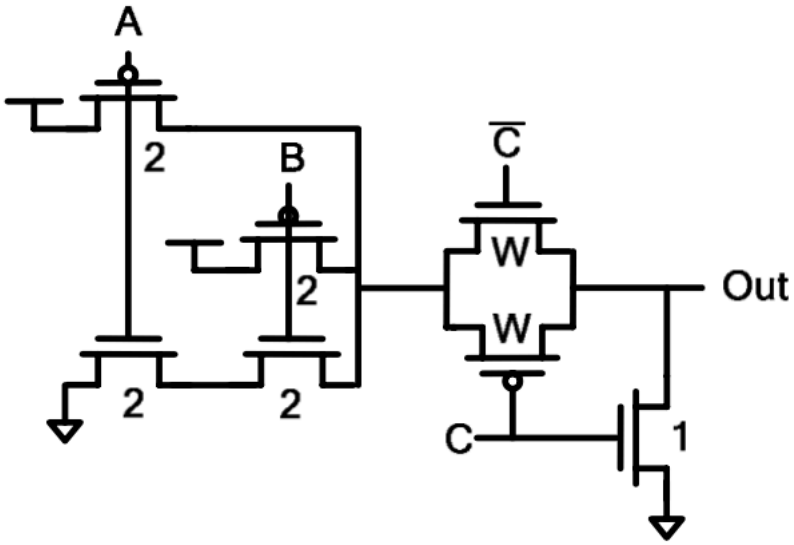


Fig.5

6. (SRAMs)

For this problem we will be looking at a 128x128 SRAM (i.e., each wordline drives 128 cells, and each bitline has 128 cells on it), with each cell shown below. The cell's layout is 2μm tall and 2.5μm wide, and both the wordline and bitline wires are 0.1μm wide. You can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10\ k\Omega/\square$, $R_{sqp} = 20k\Omega/\square$, and that for the wordline and bitline wires, $R_w = 0.1\Omega/\square$, and $C_w = 0.2fF/\mu m$.

a) For this SRAM, what is the total capacitance on each wordline? What is the total capacitance on each bitline?

b) Assuming this SRAM works at 1GHz and V_{DD}=1.2V, how much dynamic power is consumed due to the capacitance of the wordlines and bitlines?

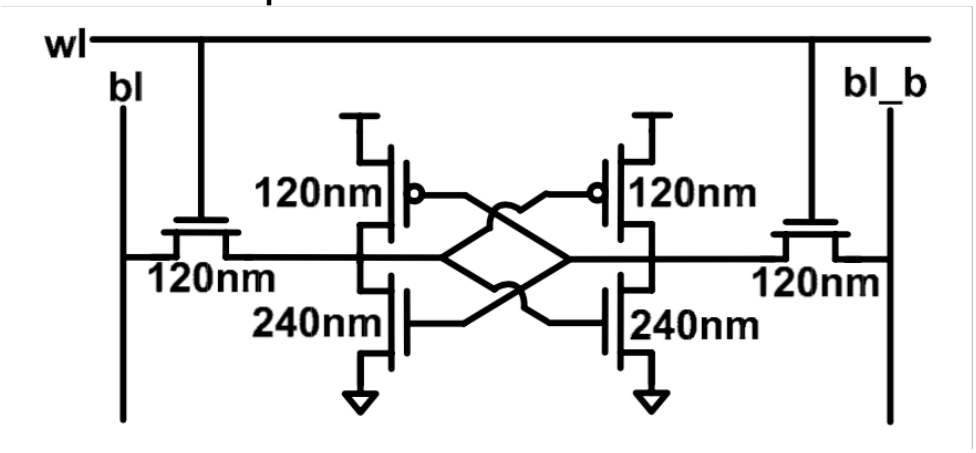
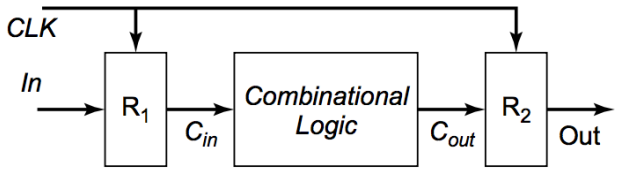


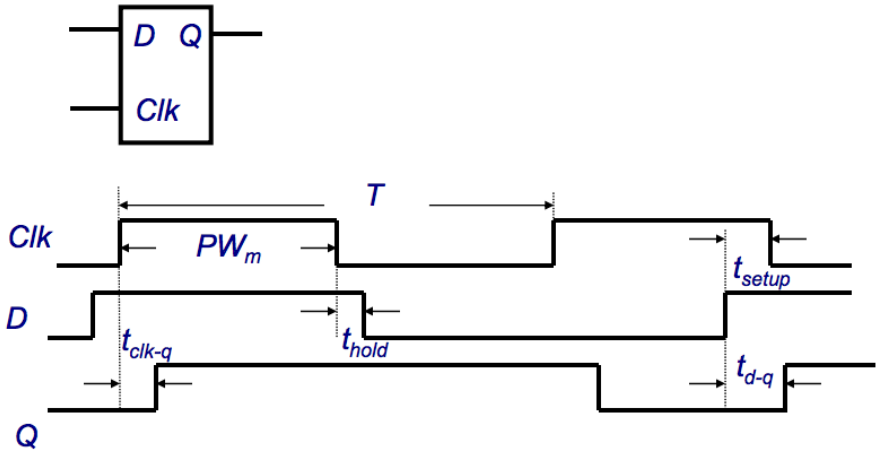
Fig.6

7. (Timing and Clock Distribution) (Bonus)
This problem set is not covered by lecture. However, it is worthy to learn since it explains timing constraints and clock uncertainties that usually are the key point when we solve the real world problem. There is the materials and definitions of the knowledge which may be used when solve this problem.

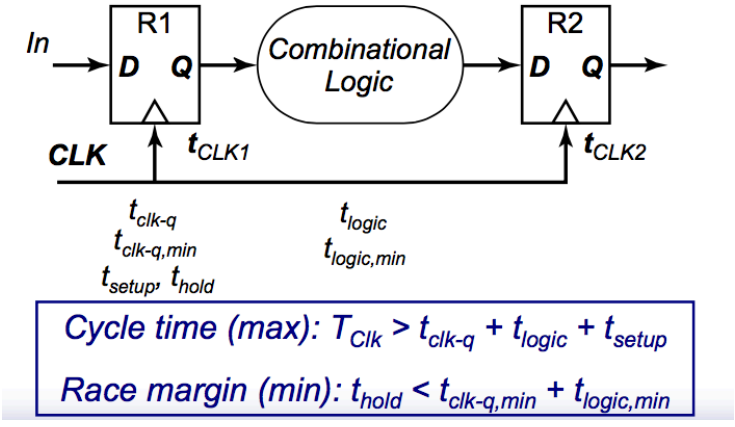
Materials and definitions:
1) Synchronous timing:



2) Latch parameters:



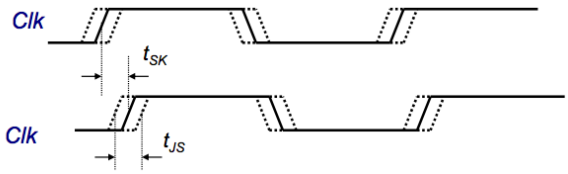
3) Timing Constraints:



4) Clock Non-idealities
①Clock skew: Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}.
②Clock jitter: Temporal variations in consecutive edges of the clock signal;

modulation + random noise; Cycle-to-cycle (short-term) t_{JS}; Long term t_{JL}.

Clock Skew and Jitter



Both skew and jitter affect the effective cycle time.
Only skew affects the race margin (usually).

Problem set:

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{clk\text{-}q}$ = 50ps, t_{setup} = 50ps, and t_{hold} = 50ps. You can assume that the clock has no jitter.

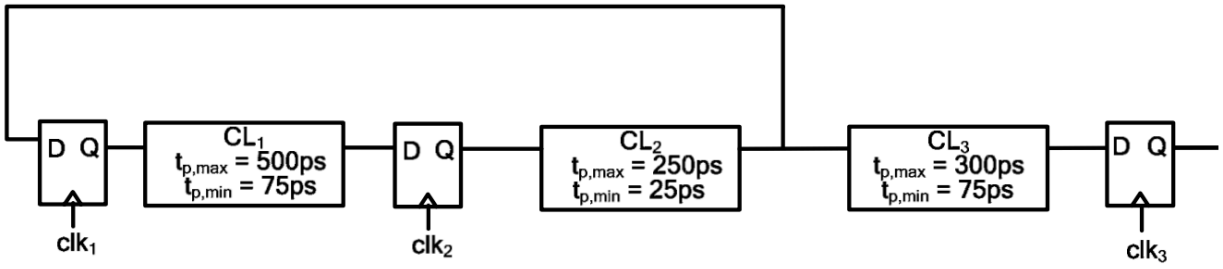


Fig.7 a

a) Assuming there is no skew between clk1, clk2, and clk3, what is the minimum clock cycle time for this pipeline? Is there any minimum delay (hold time) violations?

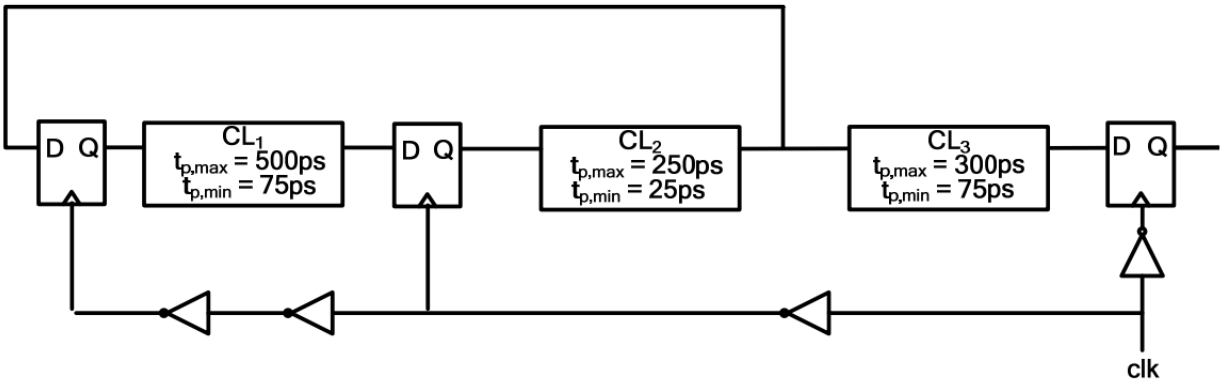


Fig.7 b

b) Now we'll include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 50ps, but that each inverter's delay varies randomly by +/-10%, now what is the minimum clock cycle time?