ESE 566A: Modern System-on-Chip Design

Homework 2

Due: Jan 30, 2:30 pm

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1. (Flip-flop Timing)

For the following clocked sequential circuit Fig.1 with one input (X) and one output (Z):

a) Drive a state table and draw a state diagram for the circuit.

b) Redesign this circuit by replacing the Q1 flip-flop (i.e. the D flip-flop holding Q1 state) with a JK flip-flop, and the Q2 flip-flop with a T flip-flop. Only show the excitation equations (or state equations) for J1, K1, and T2.

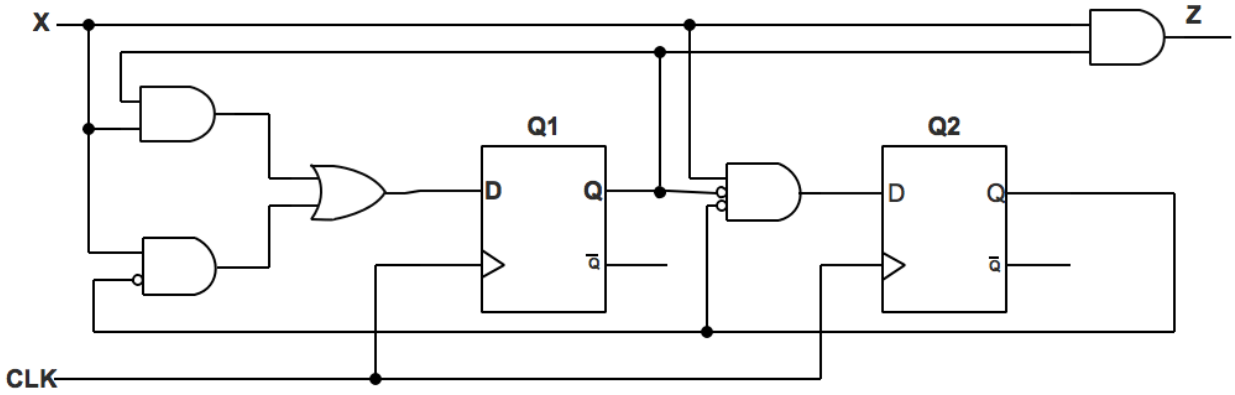

Fig.1

2. (CMOS Device Voltage Transfer Characteristic (VTC))

Using the parameters given, calculate the current through two NMOS transistors in series (see Fig. 2), when the drain of the top transistor is tied to V_{DD}, the source of the bottom transistor is tied to V_{SS} = 0, and their gates are tied to V_{DD}. The substrate is also tied to V_{SS} = 0V. Assume that W/L=10 for both transistors and L = 4μm.

K = 168μA/V^2 V_{T0} = 0.48V γ = 0.52V$^{1/2}$ $|2\phi_F|$ = 1.01V

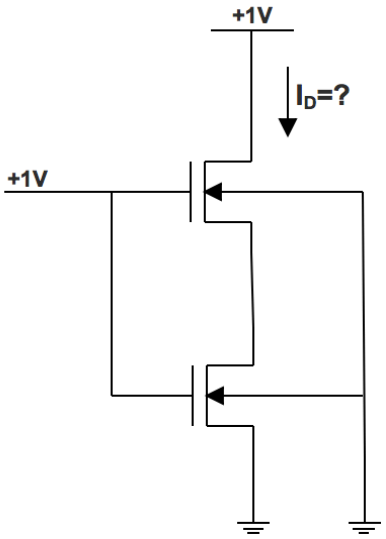

Fig.2

3. (Combinational Logic)

1. For the gate shown in Fig. 3,

Pull-up transistor ratio is 5/5

Pull-down transistor ratios are 100/5

V_{Tn} = 0.53V

V_{Tp} = 0.51 V

g = 0.574 $V^{1/2}$

$|2\phi_F|$= 1.020 V

$\frac{1}{\lambda}$ = 1.8 V

a) Identify the worst-case input combination(s) for V_{OL}.

b) Calculate the worst-case value of V_{OL}. (Assume that all pull-down transistors have the same body bias and initially, that $V_{OL} \approx 5\% V_{DD}$.)

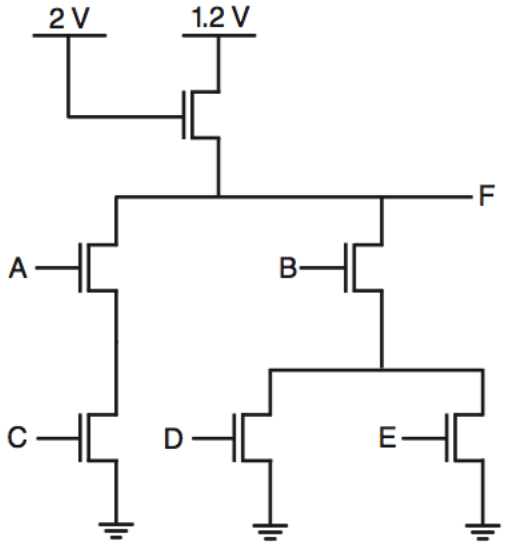

Fig.3

4. (CMOS Device Capacitance)
Consider a layout of an NMOS transistor shown in Fig. 4. The process parameters are shown below.
$N_D = 2 \cdot 10^{20} cm^{-3}$
$N_A = 2 \cdot 10^{20} cm^{-3}$
$X_j = 32nm$
$L_D = 10nm$
$t_{ox} = 1.6nm$
$V_{T0} = 0.53V$
Channel stop doping equals to 16.0 $*$ (p-type substrate doping). Find the effective drain parasitic capacitance when the drain node voltage changes from 1.2V to 0.6V.

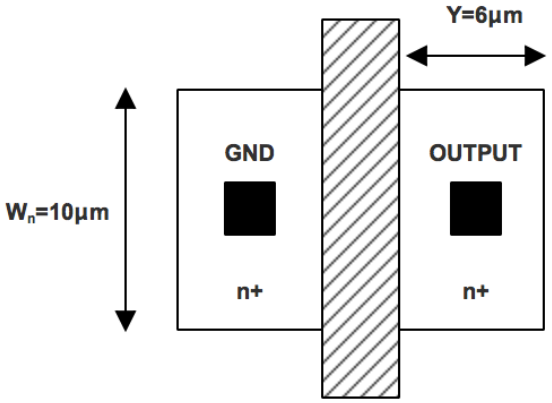

Fig.4

5. (VTC and Noise Margin)

In this problem we will analyze the noise margins for a chain of gates. For this problem, VDD = 2.5V. Fig.5 b. is a VTC for all three of the inverters in Fig. 5 a. The VTC has four segments, with a transient region between the two flat regions that can be approximated with two second-order curves.

a) Add the voltage sources to Fig.5 a that you would use for modeling noise coupling to the input and output of gate M_2. You should arrange these voltage sources so that they would both impact the noise margin in the same way (i.e., if the voltage source at the input decrease the noise margin, the voltage source at the output should also decrease the noise margin).

(Draw the voltage sources that you added on Fig.5 a directly.)

b) Determine the noise margins for gate M_2 when noise couples only to its input. (Hint: Use the information in Fig.5 b)

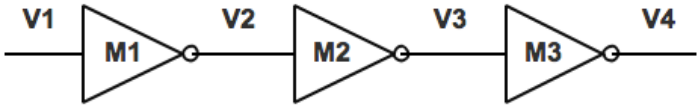

Fig.5 a

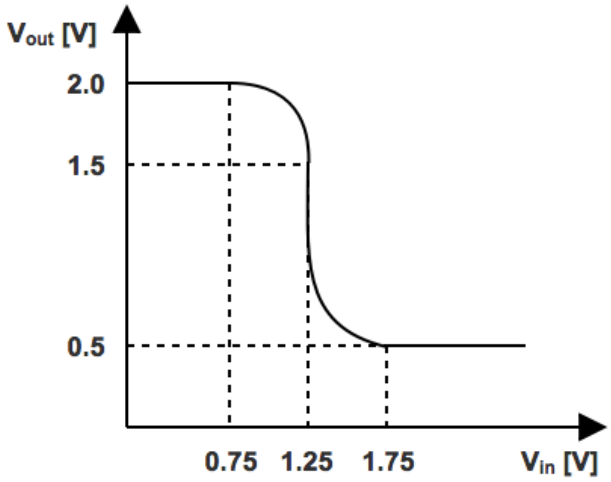

Fig.5 b

c) The following piecewise equation describes the VTC of a circuit. Is this a digital gate? Why or why not? As part of your answer, you should sketch the VTC of this gate.

$$V_{out} = \begin{cases} 2.5V & 0.0V \leq V_{in} < 0.5V \\ 2.5V - 4(V_{in} - 0.5V)^2 & 0.5V \leq V_{in} < 1.0V \\ 2.5V - V_{in} & 1.0V \leq V_{in} < 1.5V \\ 4(V_{in} - 2V)^2 & 1.5V \leq V_{in} < 2.0V \\ 0V & 2.0V \leq V_{in} < 2.5V \end{cases}$$

6. (Propagation Delay)
Consider the CMOS circuit shown below.

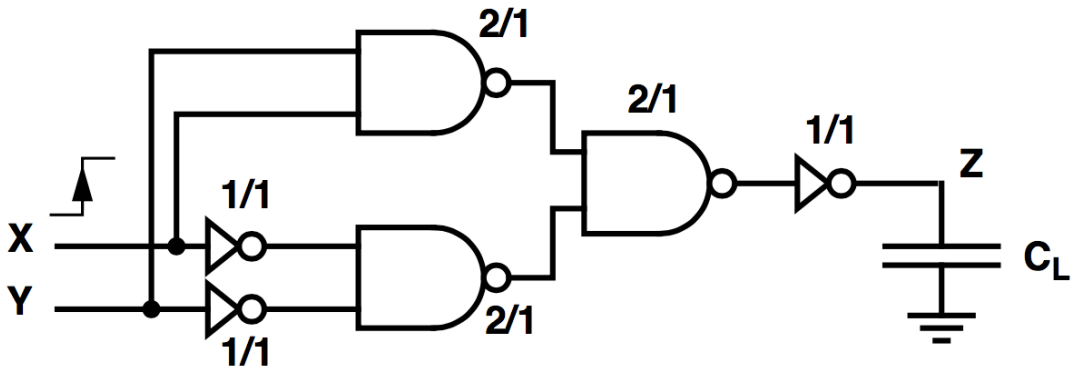

Fig.6

In the figure, the W/L ratios for each gate apply to both NMOS and PMOS transistors. (i.e., 2/1 on top of the top NAND means the W/L of top NAND is 2/1) We want to determine the delay from a rising transition (0 → 1) on input X to the output Z. Let us denote by $\tau = R_nC_n$ the product of the effective on-resistance and gate capacitance of the minimum-sized NMOS transistor, i.e. $(W/L)_n = 1/1$. For the minimum-sized PMOS transistor, we have $R_p = 2R_n$. Also, the output Z drive load is $C_L = 10C_n$.

a) Assuming that the rise and fall times are good approximations of the propagation delay, determine the delay from X to Z, in terms of , τ when Y = 0.

b) Now, assume that Y = 1. What is the new value for the propagation delay from X to Z? Can you comment on this?

7. (Complex CMOS Gates)

a) Implement the function. $F = \overline{A} \cdot \overline{B} + \overline{C} + \overline{D}$. Assuming long-channel transistors, size the devices so that the drive resistance is the same as an inverter with $W_N/L = 2$ and $W_P/L = 4$.

b) Imagine that input "A" to the gate was always the last one to arrive, making the delay of the gate from A rising or falling to the output falling or rising critical. Please re-arrange the implementation of your gate so that the delay of the gate from A transitioning is minimized.