Tutorial for Encounter

STEP 1: Login to the Linux system on Linuxlab server. Start a terminal (the shell prompt). (If you don't know how to login to Linuxlab server, look at here)

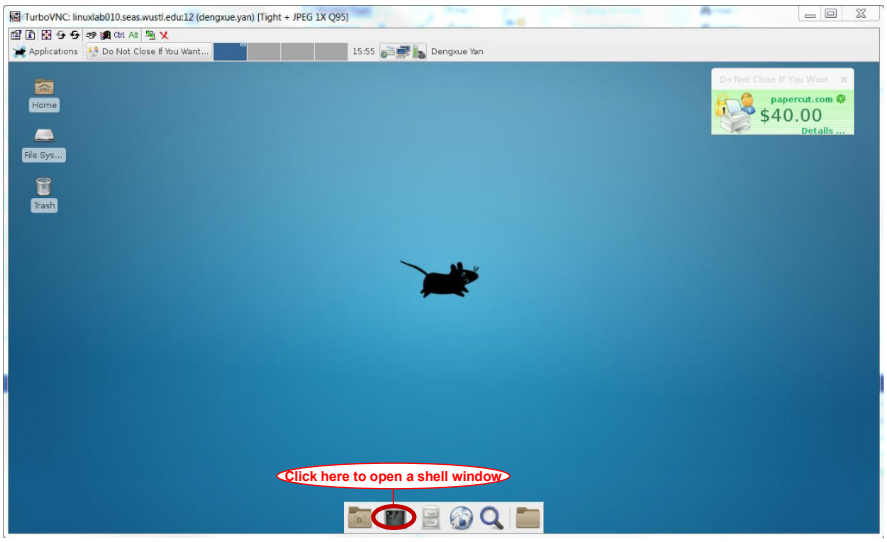

Fig. 1 The screen when you login to the Linuxlab through equeue

STEP 2: Build work environment for class ESE461.

In the terminal, execute the following command:

module add ese461

This command will build work environment for class ESE461. You could perform "*module avail*" in the terminal to find the available modules on Linuxlab before you do "*module add ese461*" . Make sure ese461 is presented when you execute this command.

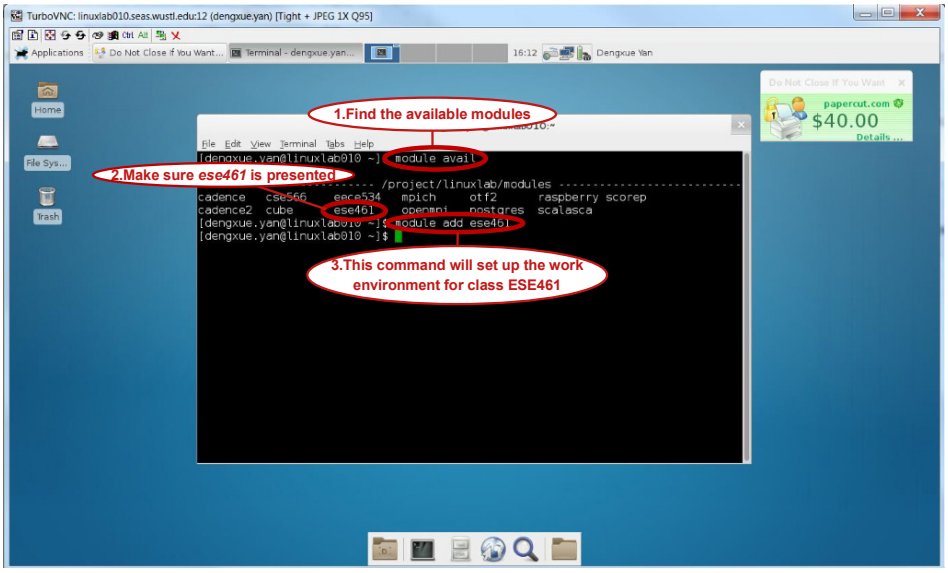

Fig. 2 Build work environment for class ESE461 using module

STEP 3: In the terminal, change path to your project directory, and compile your code using design compiler.

(If you don't know how to use design compiler, look at here)

STEP 4: Download the "*Default.view*" and modify it according to your design for MMMC view definition file later. Please specify the name of the .sdc file used in your synthesis script. It should be the .sdc file generated by Design Compiler in the previous design step.

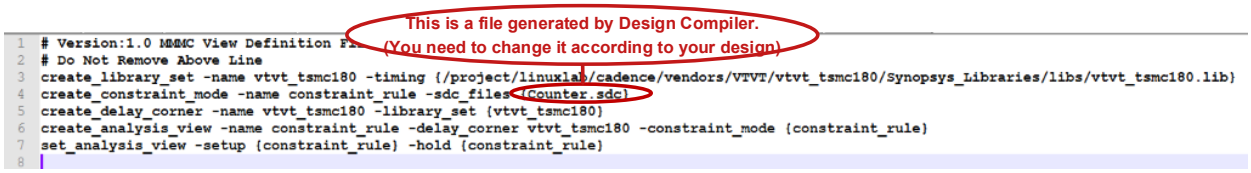

Fig. 3 Default.view

STEP 5: Then execute the following command in the shell to start *encounter*:

encounter

You will get the following printout in the terminal and a window pops up which looks like the one as below. This window will lead to the design window.

Fig. 4 Command and the printout of "encounter"

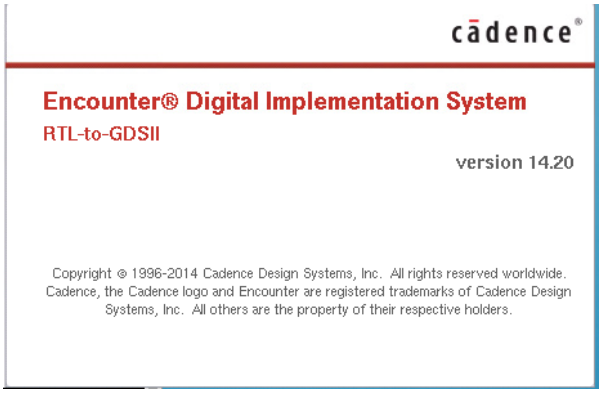

Fig. 5 The window popped out when execute "encounter"

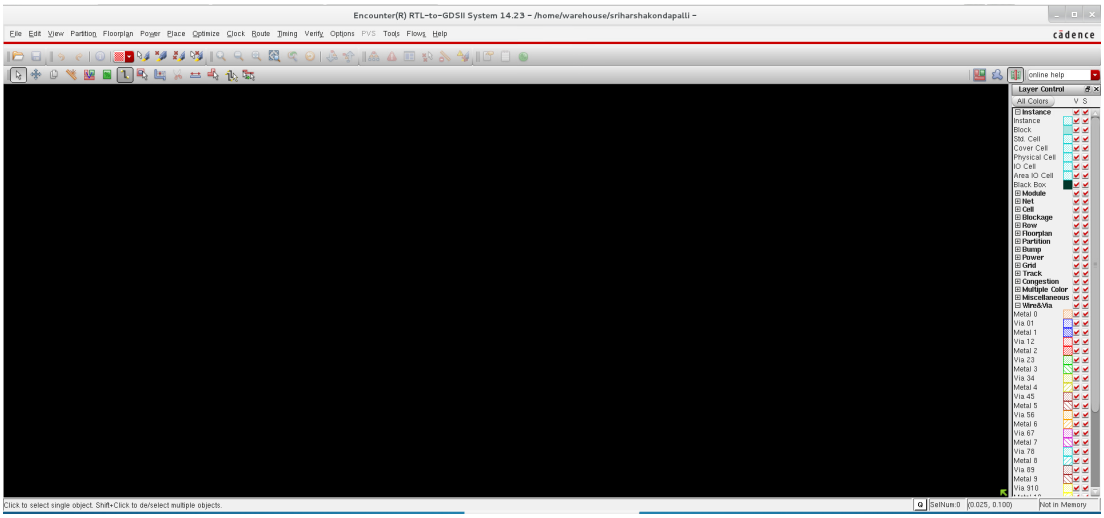

Fig. 6 The design window of "encounter"

STEP 6: Go to "*File->Import Design*" and add files to import your *netlist* file

1) You have to provide synthesized Verilog (*.syn.v*) which is the output *netlist* file generated by *Design Compiler* in the previous design step.
2) You have to provide path for the LEF file from technology library. Set path to "/project/linuxlab/cadence/vendors/VTVT/vtvt_tsmc180/vtvt_tsmc180_lef" and select the "vtvt_tsmc180.lef" file from the folder.
3) Also provide the supply nets as vdd! and gnd! in the appropriate boxes as below. These represent the global power supply and ground net in your design.
4) Load the "Default.view" edited above for MMMC view definition file
5) Click "OK" to finish

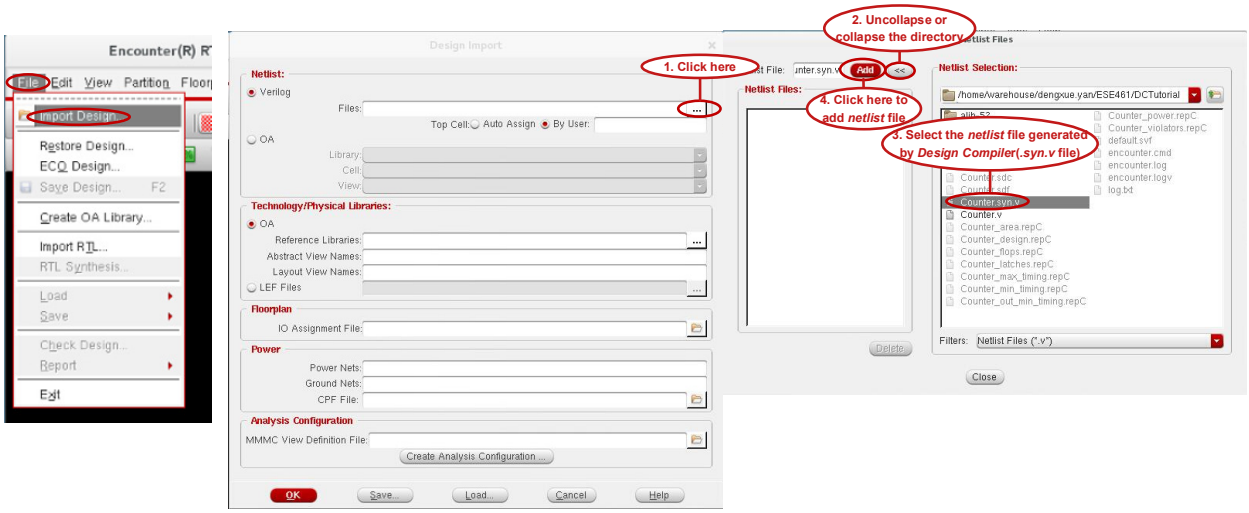

Fig. 7 Import netlist

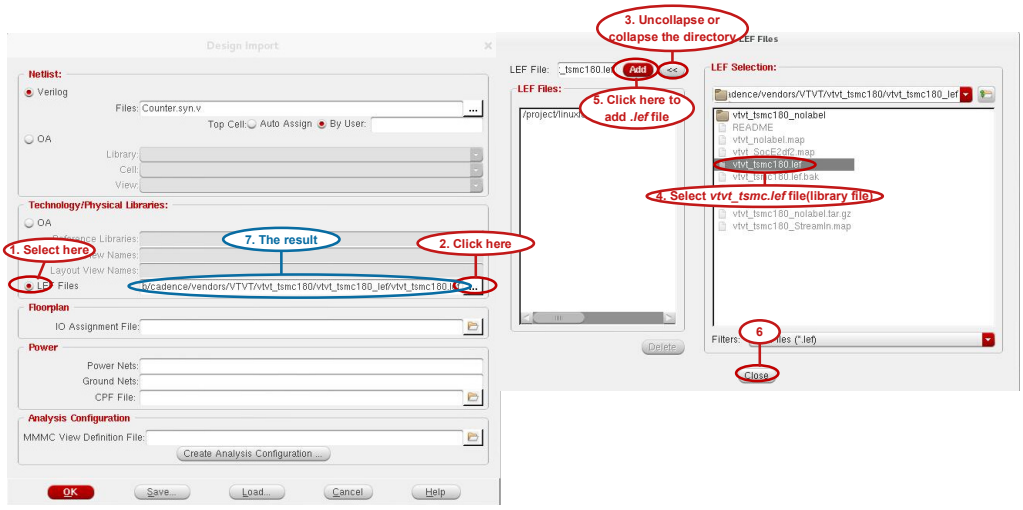

Fig. 8 Import LEF file

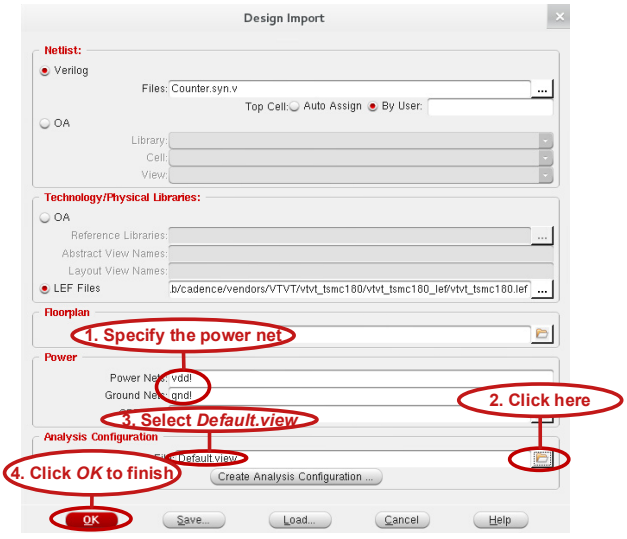

Fig. 9 Add power net and MMMC view file

STEP 7: After step 6, you will be seeing a blank screen with horizontal lines on your main window (layout window). Press "f" for fit screen view of layout.

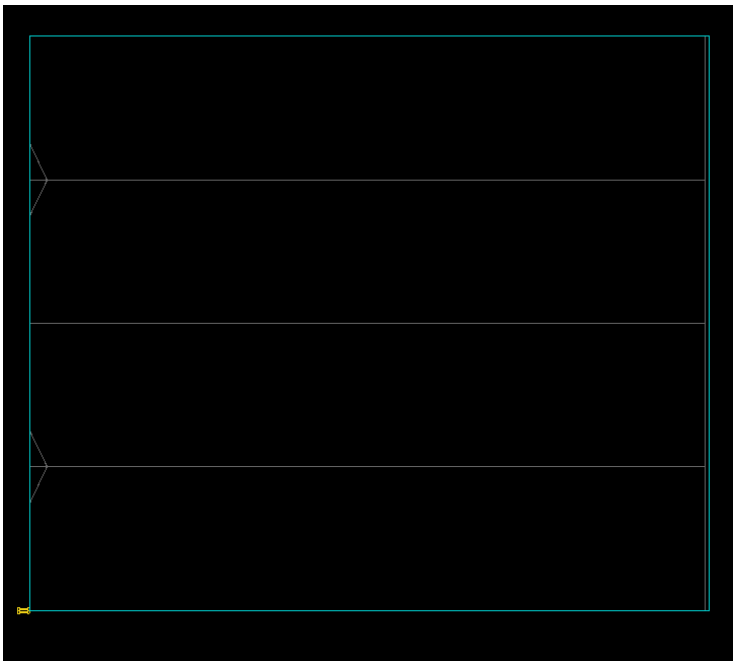

Fig. 10 The initial layout window

STEP 8: Specify "*floorplan*" options in the "*Floorplan->Specify Floorplan*" and set the values as below.

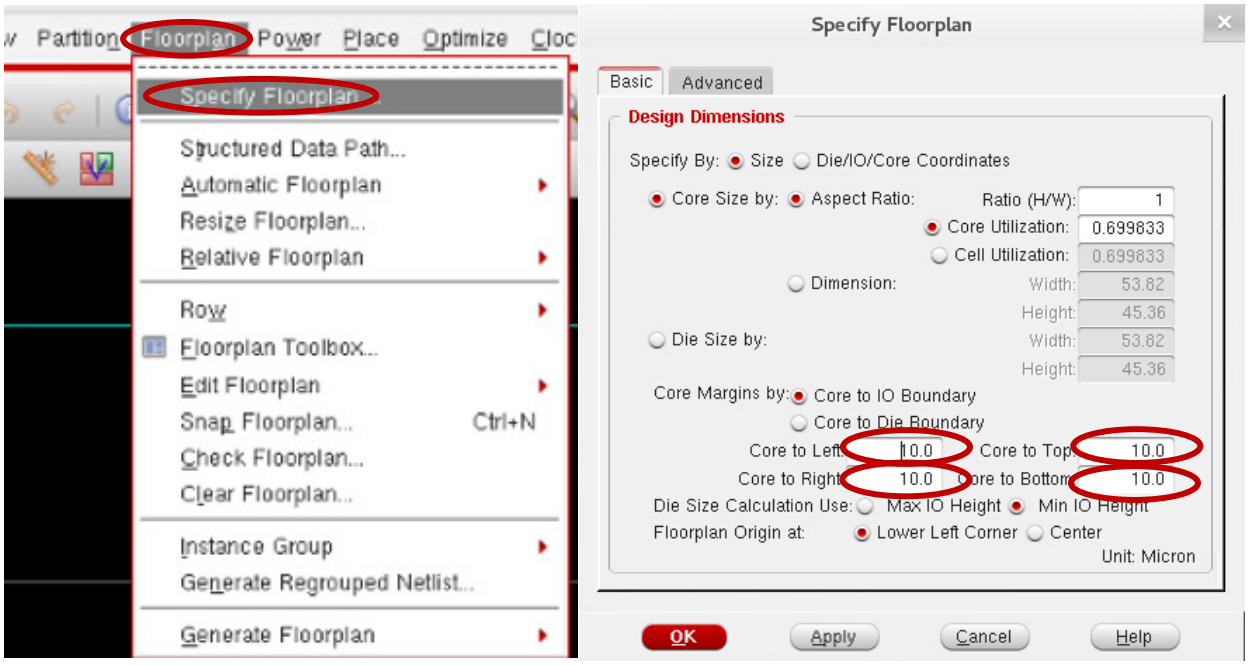

Fig. 11 Specify Floorplan

STEP 9: Set the global nets *vdd!* and *gnd!* at "*Power->Connect Global Nets*".

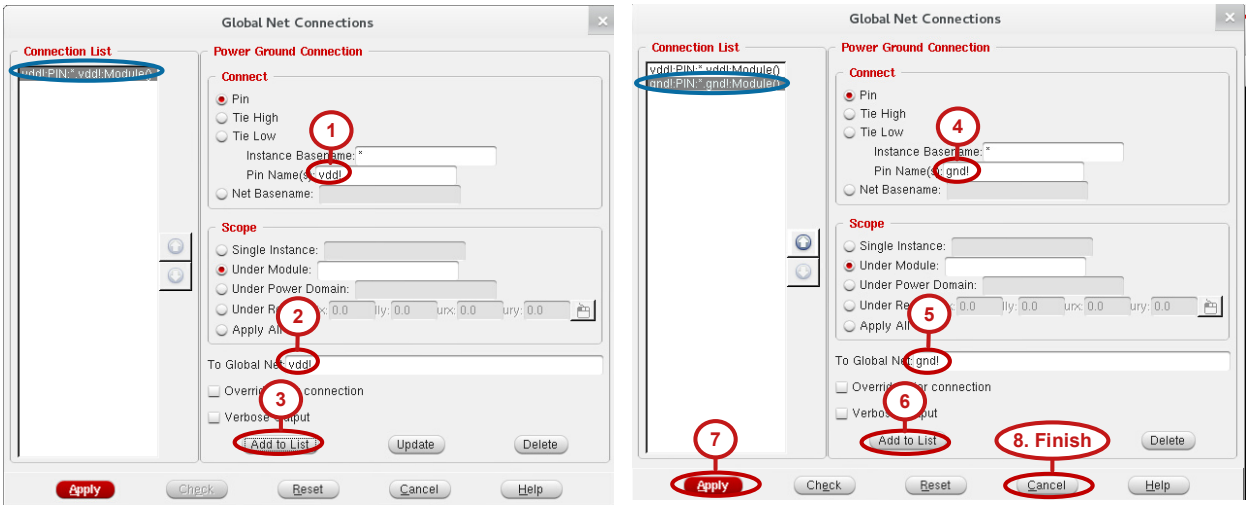

Fig. 12 Set the global nets

STEP 10: Go to "*Power->Add Ring*" and set Net pins to *vdd!*, *gnd!*. Also you change width and spacing of power ring.

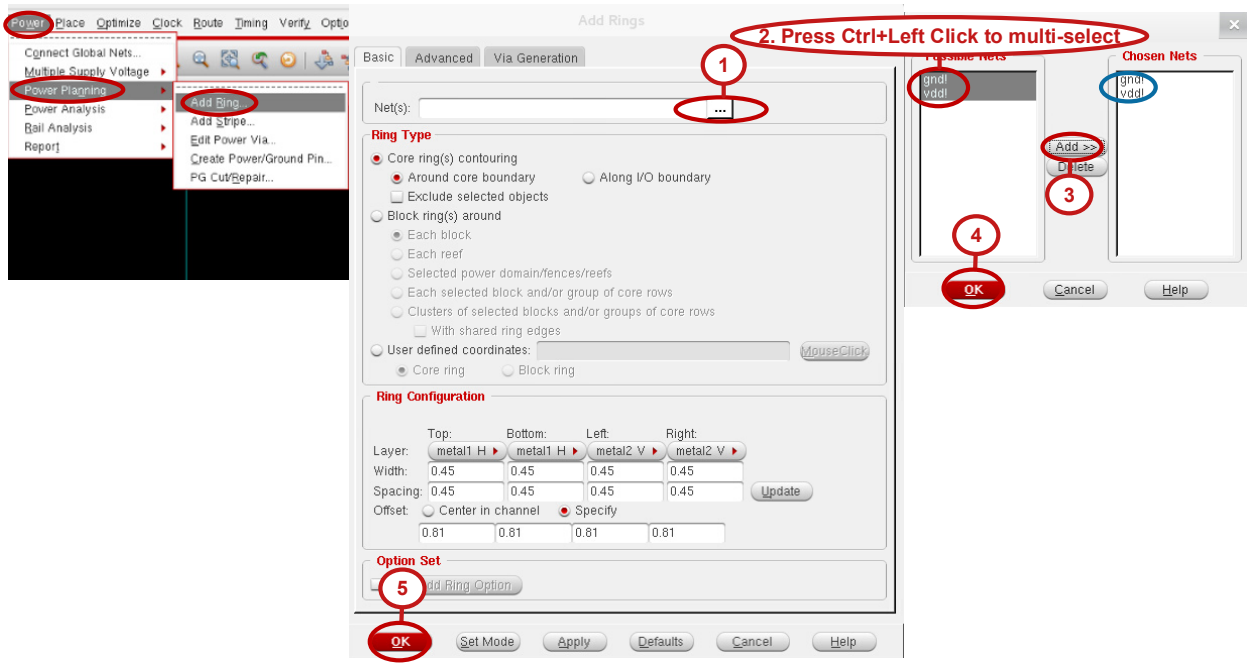

Fig. 13 Add power ring

STEP 11: We can also edit the pin placement in our design. Go to "Edit->Pin Editor". Group some pins and you can place them on left or right side of the design. If you don't specify *Encounter* will be taking appropriate placement during optimization. Once done click "OK"

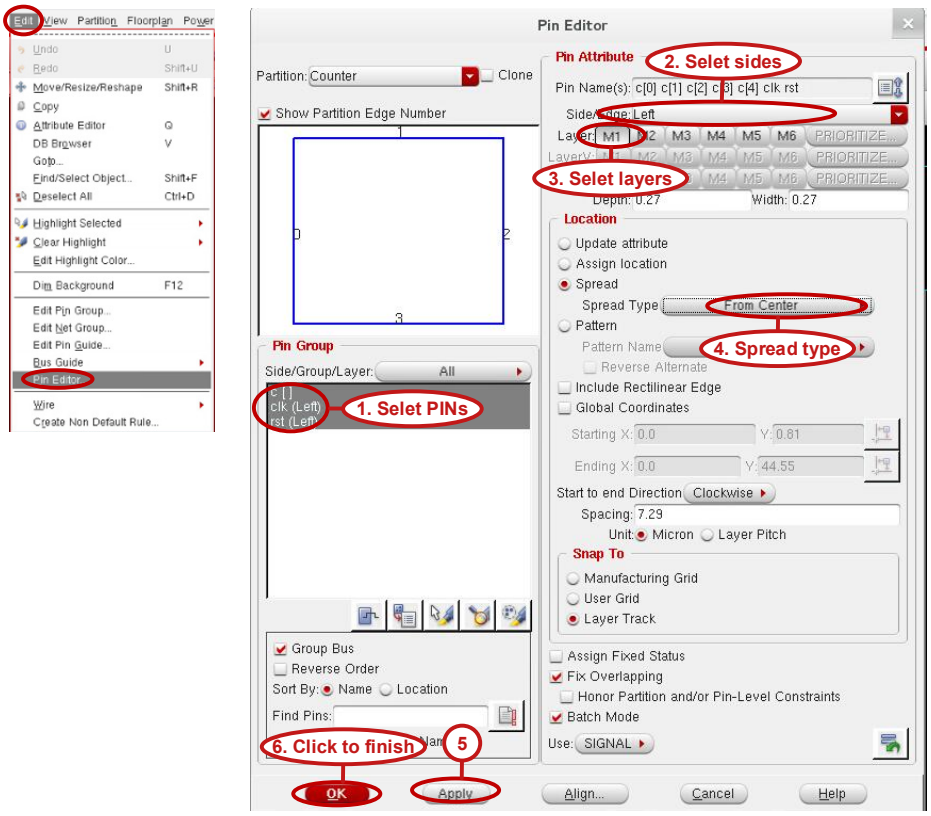

Fig. 14 Pin Editor

Watch how your layout is changing while you are setting the parameters in the GUI

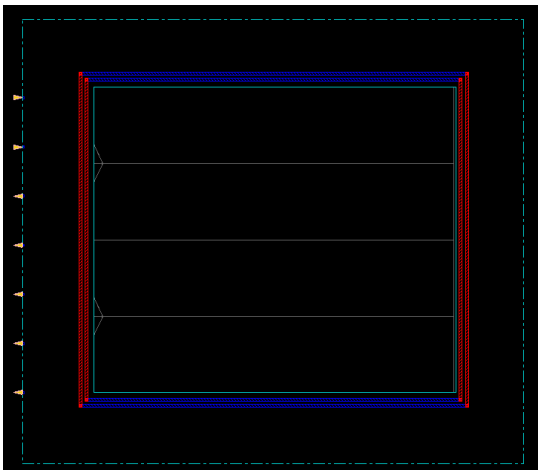

Fig. 15 The layout view after edit pins

STEP 12: Place the *vdd!* and *gnd!* in the design. Go to "*Route->Special Route*"

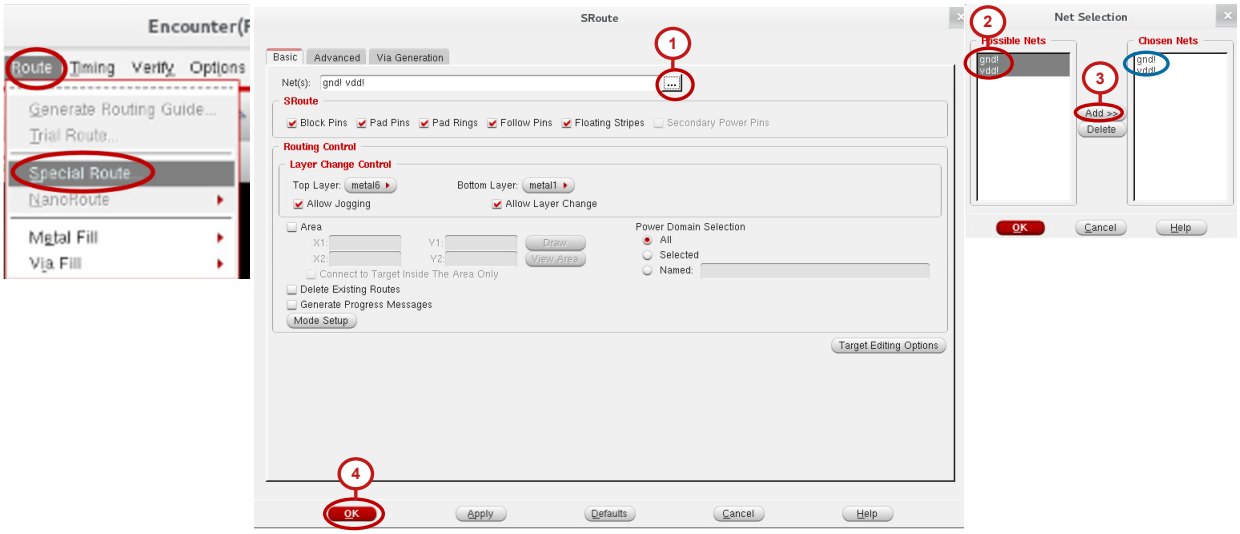

Fig. 16 Place vdd! and gnd!

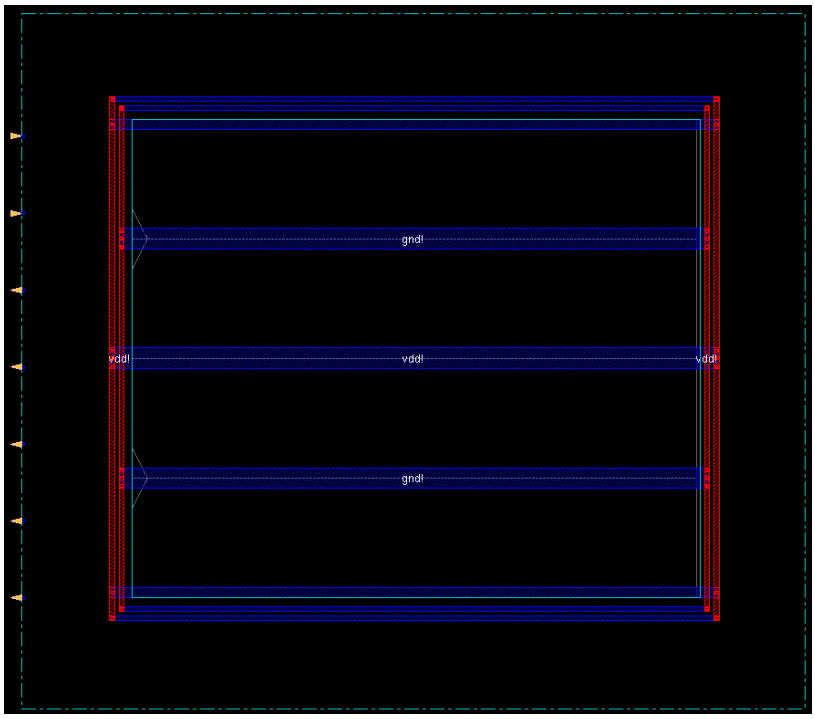

Fig. 17 The layout after place vdd! and gnd!

STEP 13: Now we are all set to place the design. So we then go to "*Place->Place Standard Cell*". Click OK.

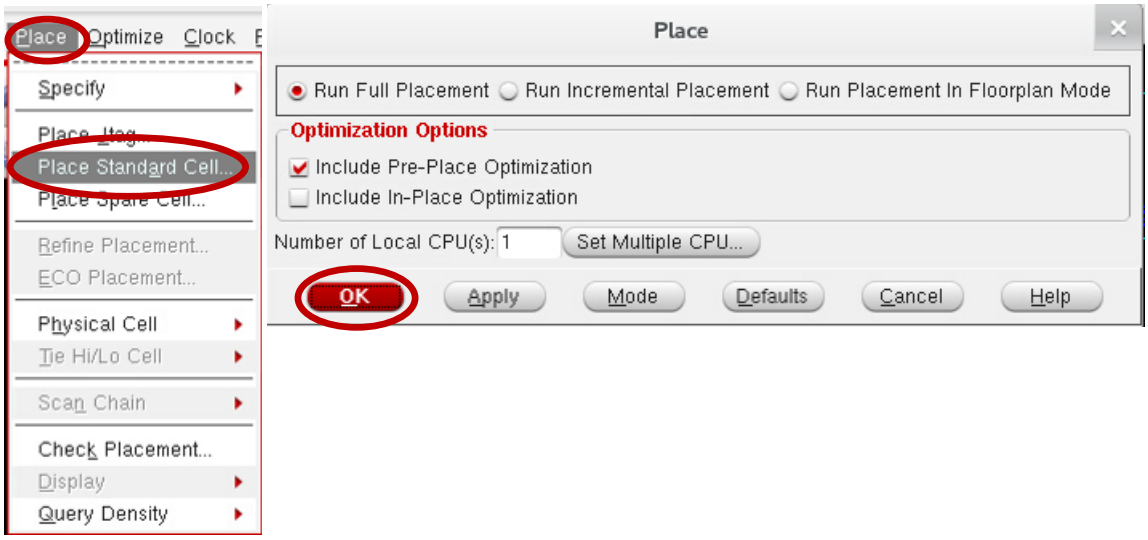

Fig. 18 Place standard cell

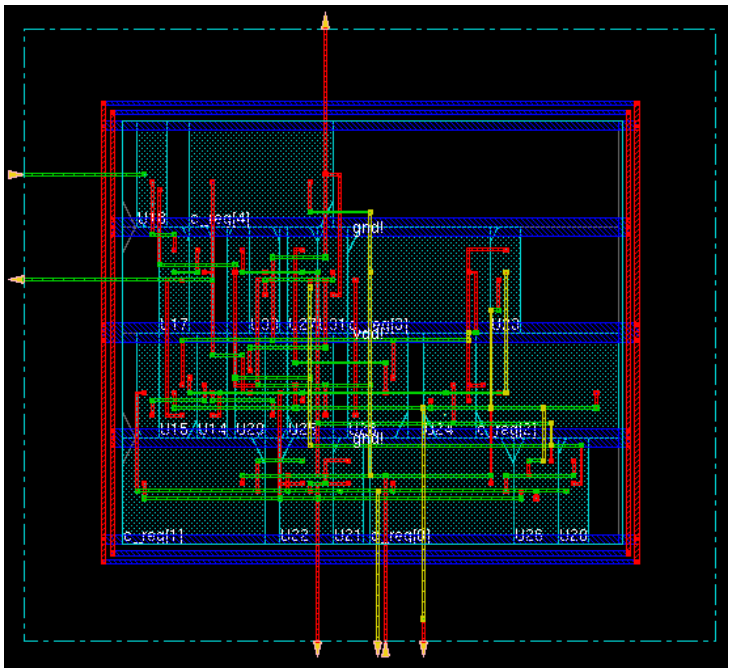

Fig. 19 The result after place standard cell

STEP 14: Clock tree synthesis:

1) Download *Clock.ctstch* and place it in working directory.
2) Download *Clock.tcl* and place it in working directory.
3) Open *Clock.tcl* using *gedit* and copy the content line by line to the *encounter terminal* and execute it.

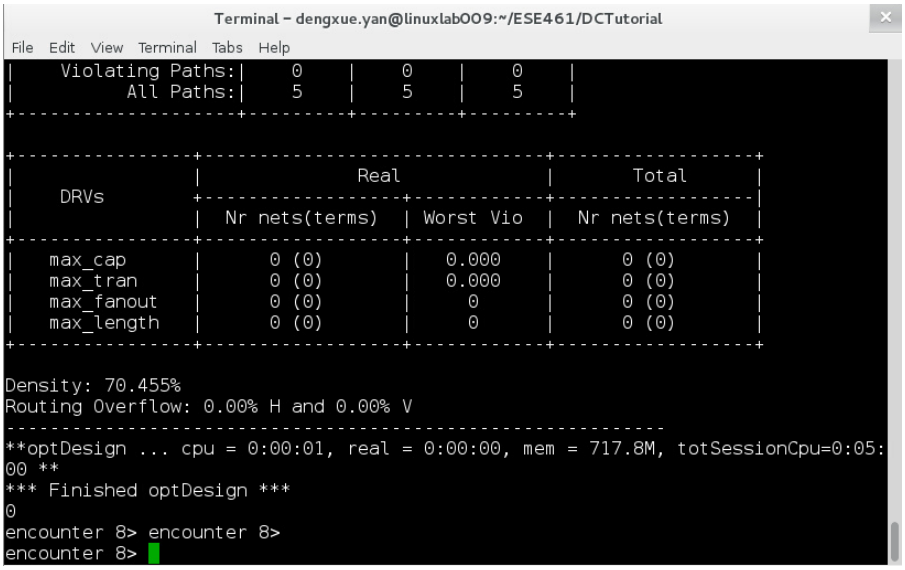

Fig. 20 Partial of clock tree synthesis commands and results

STEP 15 As part of routing go to "Route->NanoRoute->Route". And click OK.

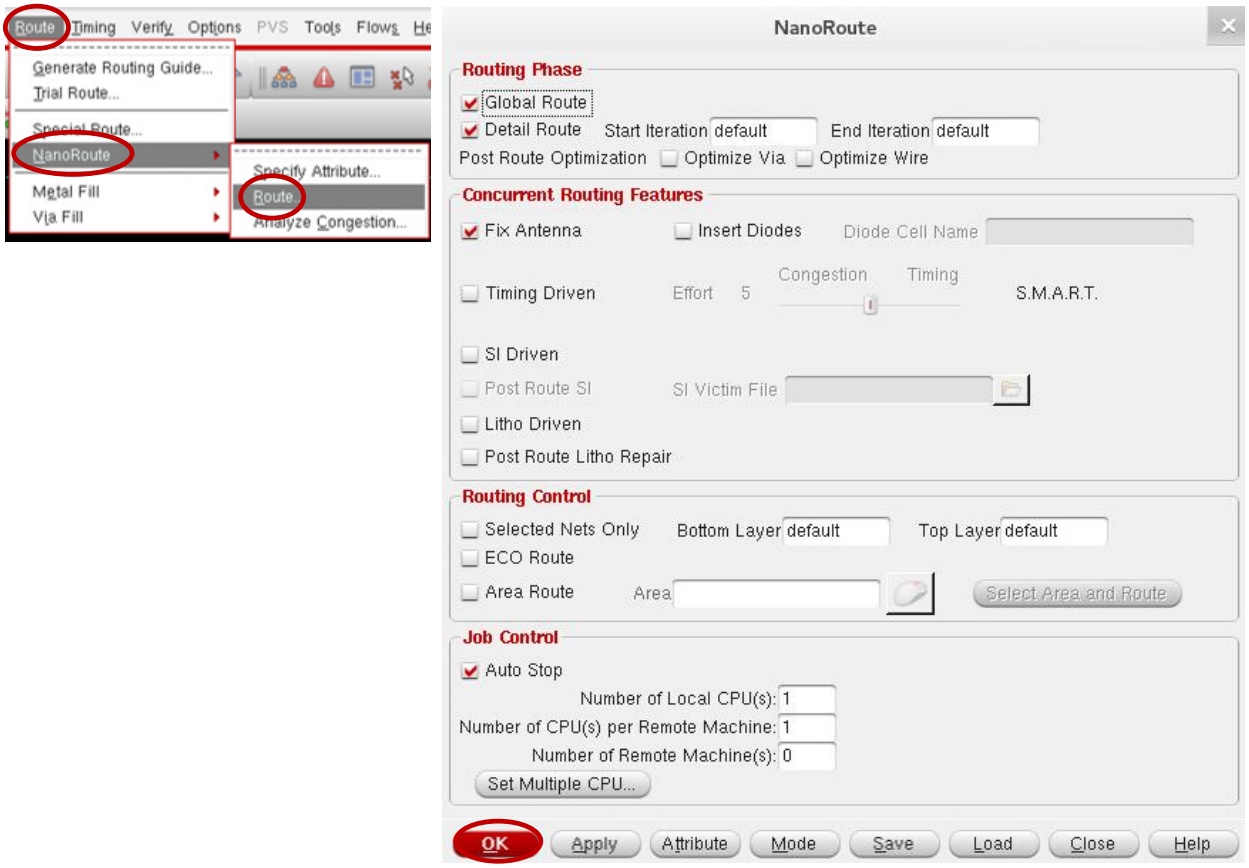

Fig. 21 Nano route

You will see that your design got placed in the layout and also all the interconnections are done.

STEP 16: Add Filler. "*Place->Physical Cell->Add Filler*". Select "filler" cell name and click OK.

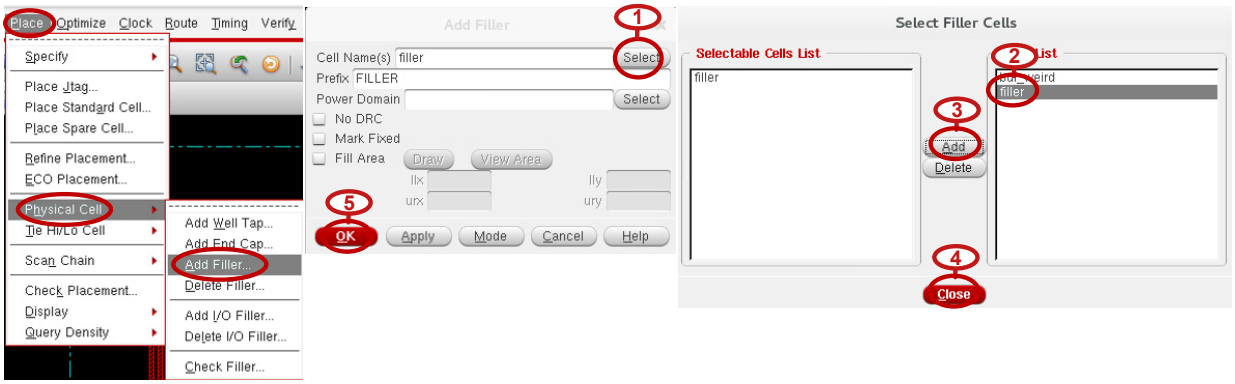

Fig. 22 Add Filler

STEP 17: Once Place and Route is done:

1) Go to "Verify->Verify Geometry". Click OK.

2) Go to "Verify->DRC". Click OK

3) Go to "Verify-> Connectivity". Click OK

Check the terminal every time for any violations and warnings.

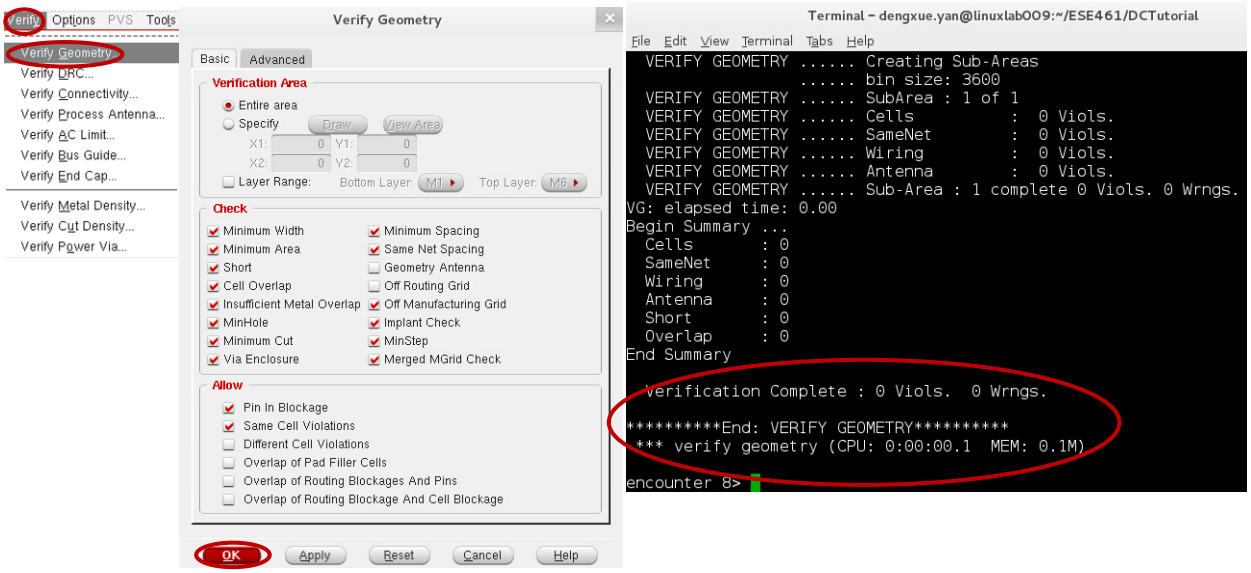

Fig. 23 Verify Geometry

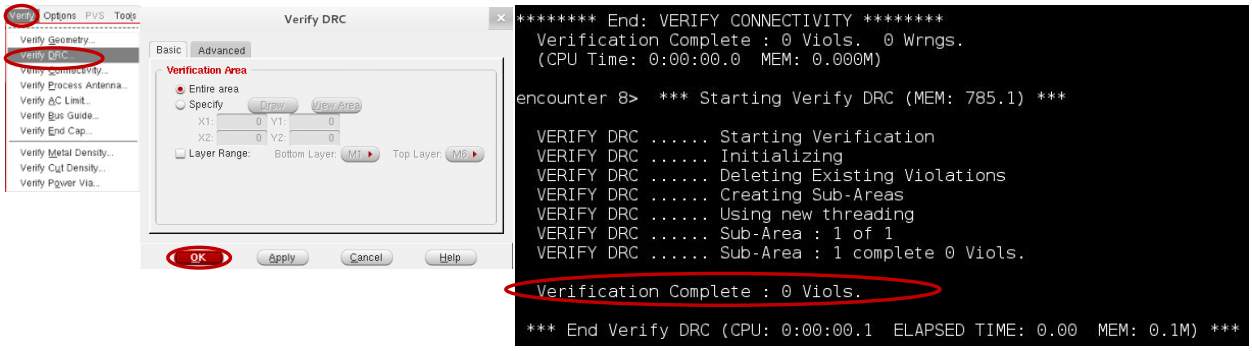

Fig. 24 Verify DRC

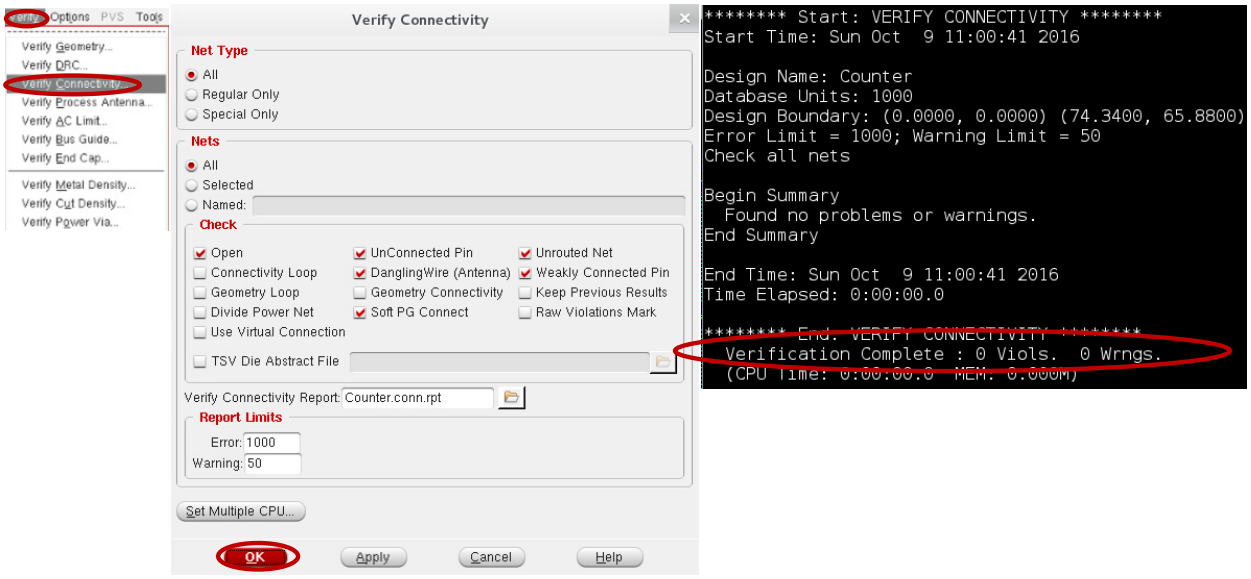

Fig. 25 Verify Connectivity

STEP 18: Generating timing report

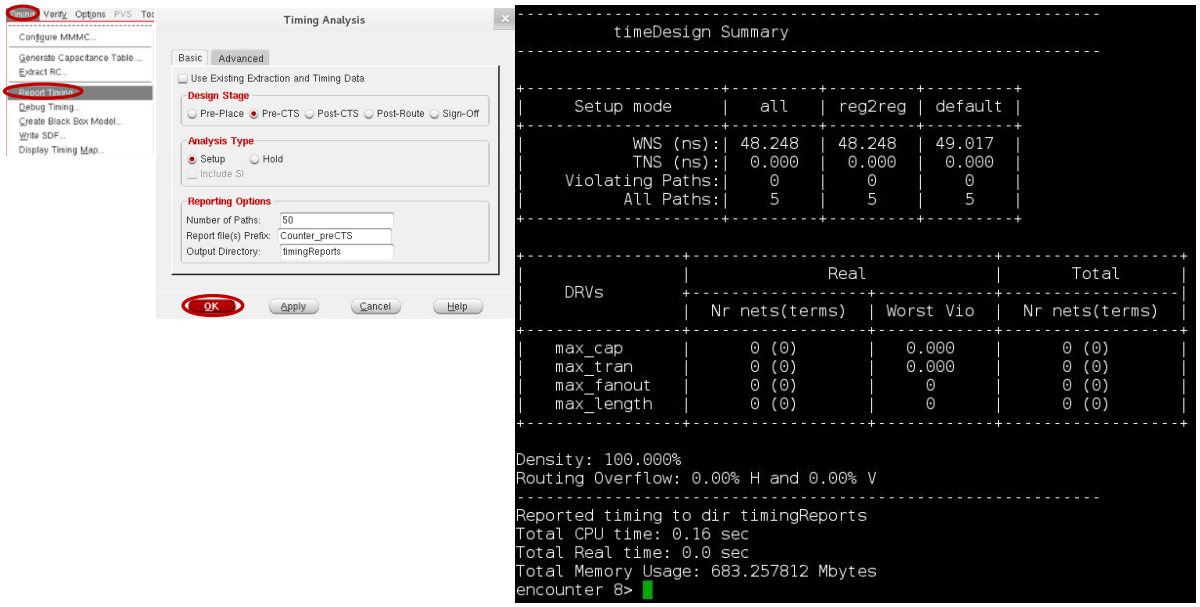

Fig. 26 Generating timing report

Additional Information for Design Compiler:

Save your design for later use. “File -> Save”. Give an output file name for each floorplan, Place, Netlist and DEF file so that you can save all the optimization options and can load it later.

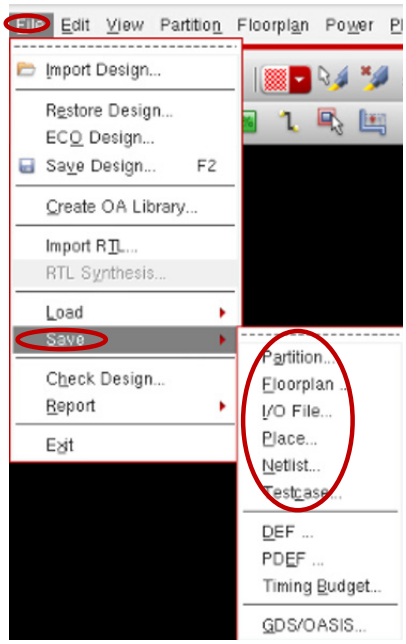

Fig. 27 Save your project