Lecture 16
Physical Design, Part 2

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http://classes.engineering.wustl.edu/ese461/

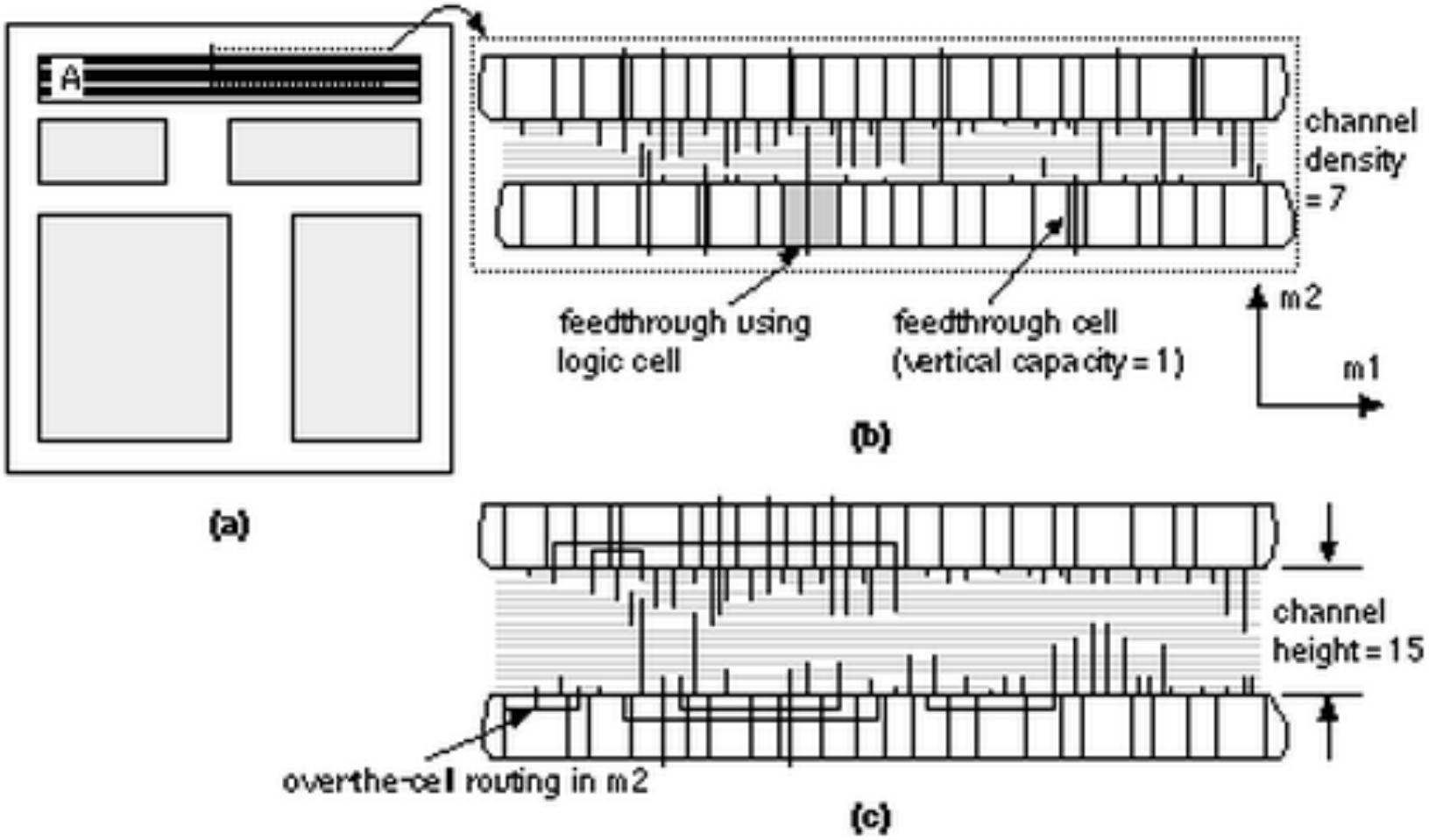
Placement

- Place logic cells within the flexible blocks
- Ideal objectives
  - guarantee the router can complete the routing step
  - minimize all the critical net delays
  - make the chip as dense as possible
  - minimize power, crosstalk between signals

- Realistic objectives
  - minimize total estimated interconnect length
  - meet the timing requirement for critical nets
  - minimize the interconnect congestion

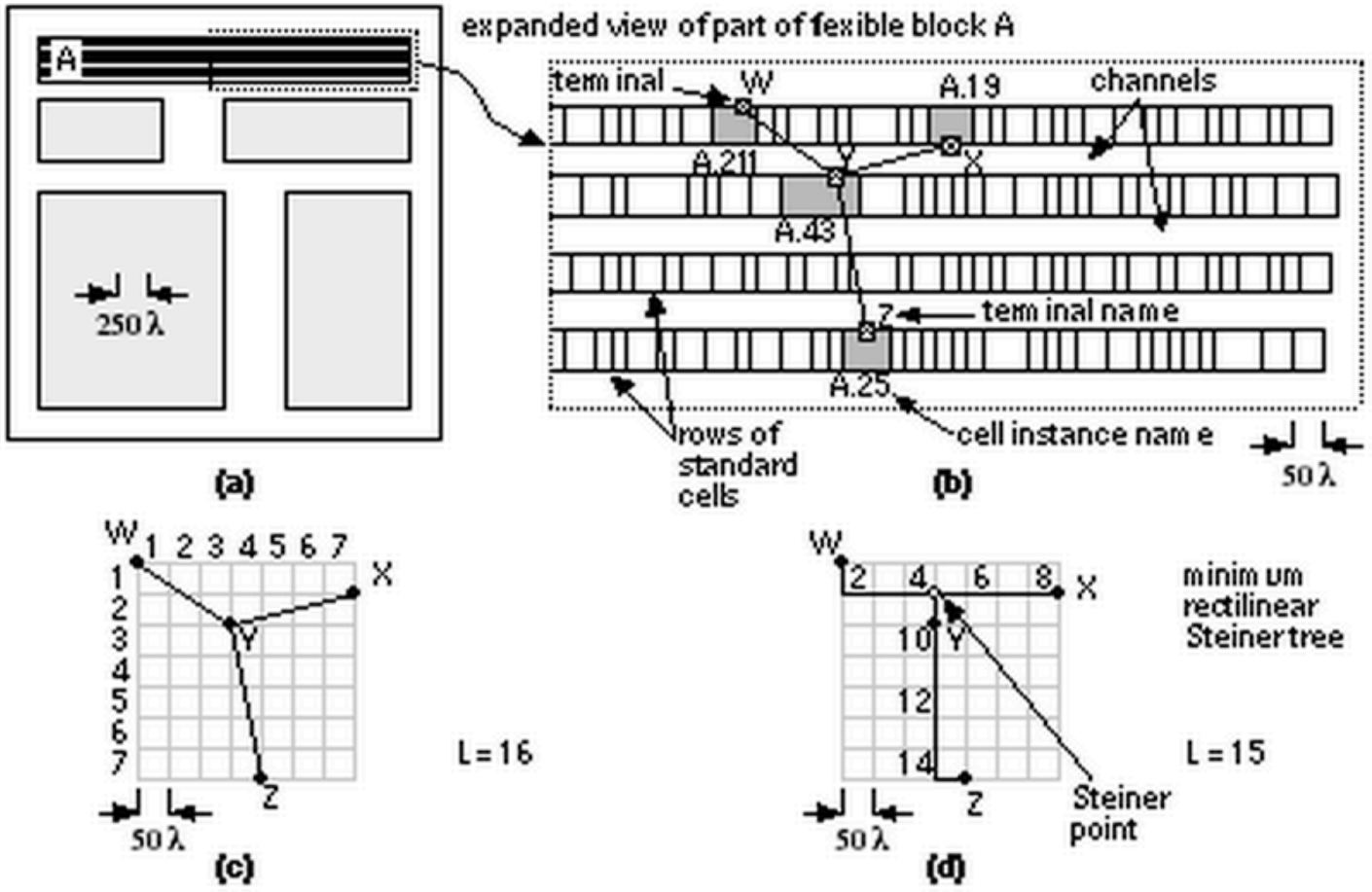
Placement Terms

- Over the cell routing (OTC)
- Channel capacity
- Feedthroughs (feedthrus)
- Jumper (unused vertical track in a cell)



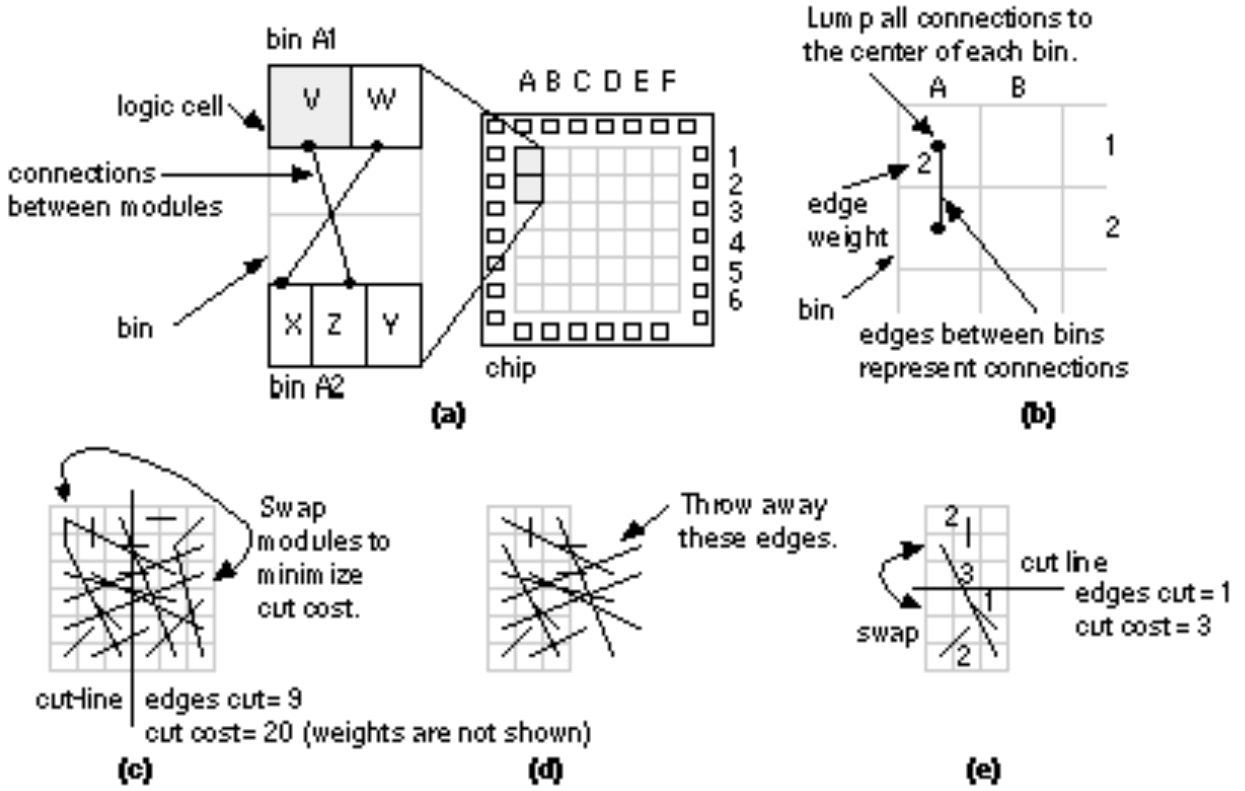
Placement Terms

- Manhattan distance vs Euclidean distance
- Minimum Rectilinear Steiner Tree (MRST)



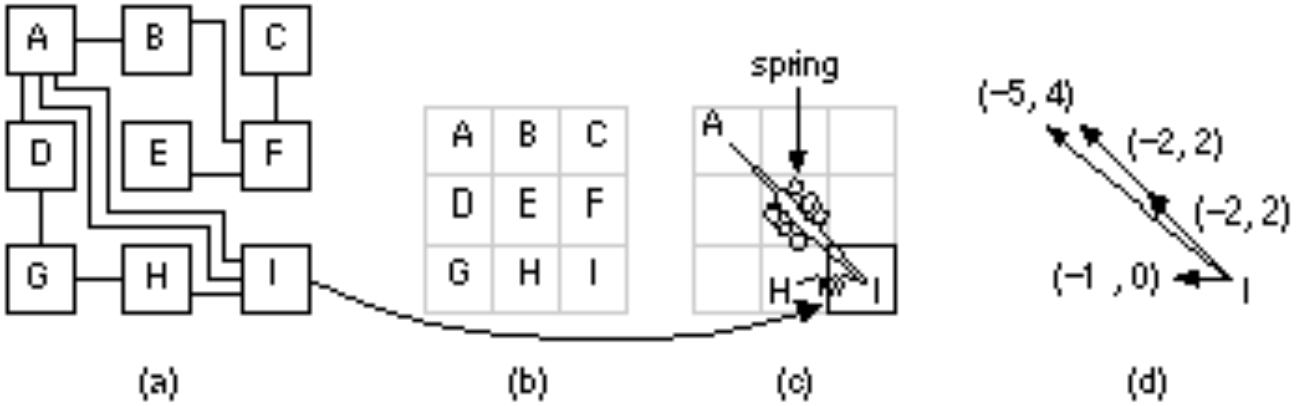
Placement Algorithms

- Constructive placement method
  - Min-cut algorithm
    - cut the placement area into two pieces
    - swap logic cells to minimize cut cost
    - repeat and cut smaller pieces till all cells placed



Placement Algorithms

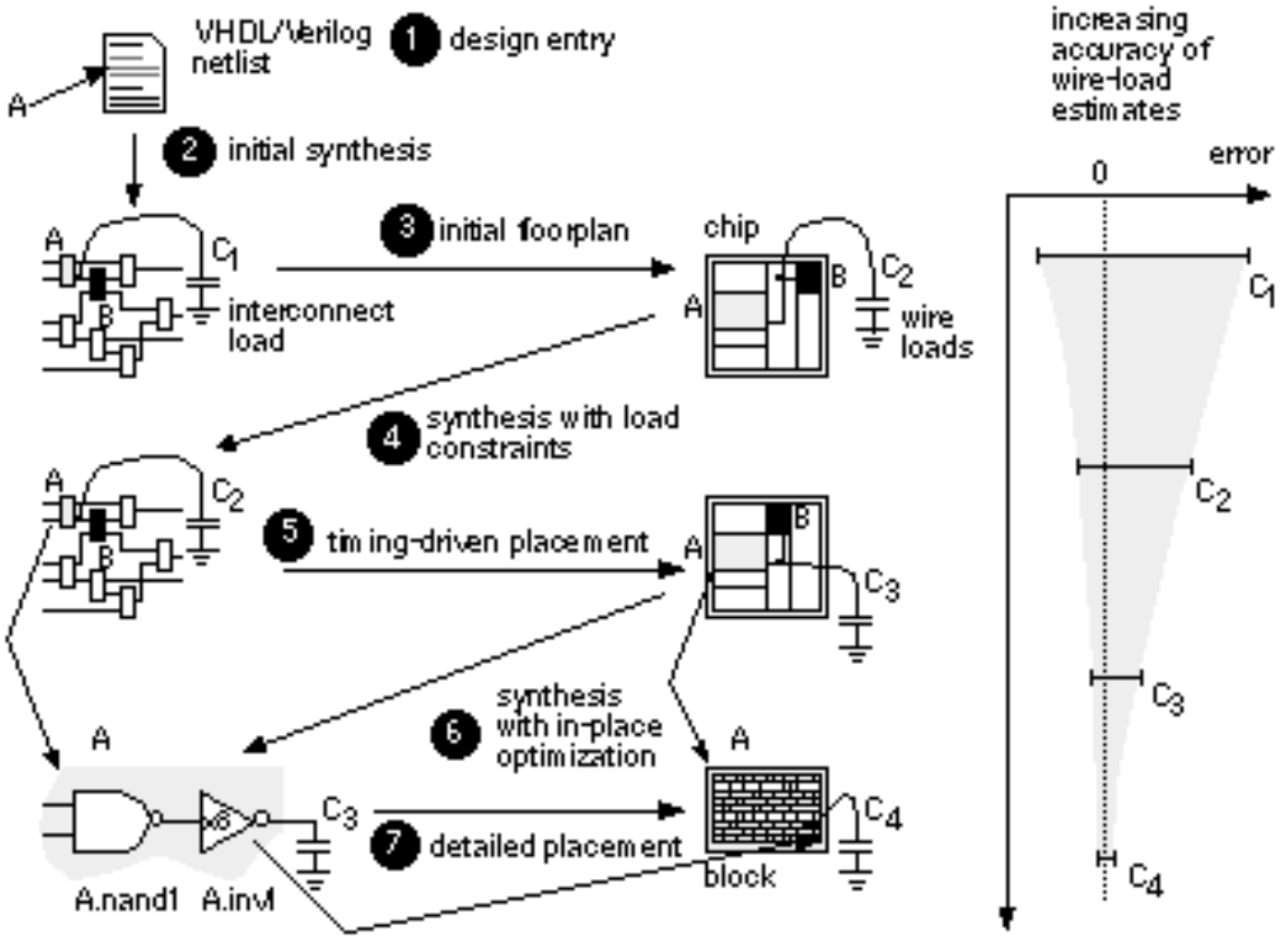
- Constructive placement method
  - Eigenvalue placement algorithm
    - cost matrix or weighted connectivity matrix
    - quadratic optimization problem
- Iterative placement method
  - take existing placement and improve it
  - pairwise interchange algorithm
  - force-directed algorithm



Physical Design Flow

- Design entry
  - logic description with no physical information
- Logic synthesis
- Initial floorplan
- Synthesis with load constraints
- Timing-driven placement
- Synthesis with in-place optimization
- Detailed placement
- Global routing
- Detailed routing

Physical Design Flow

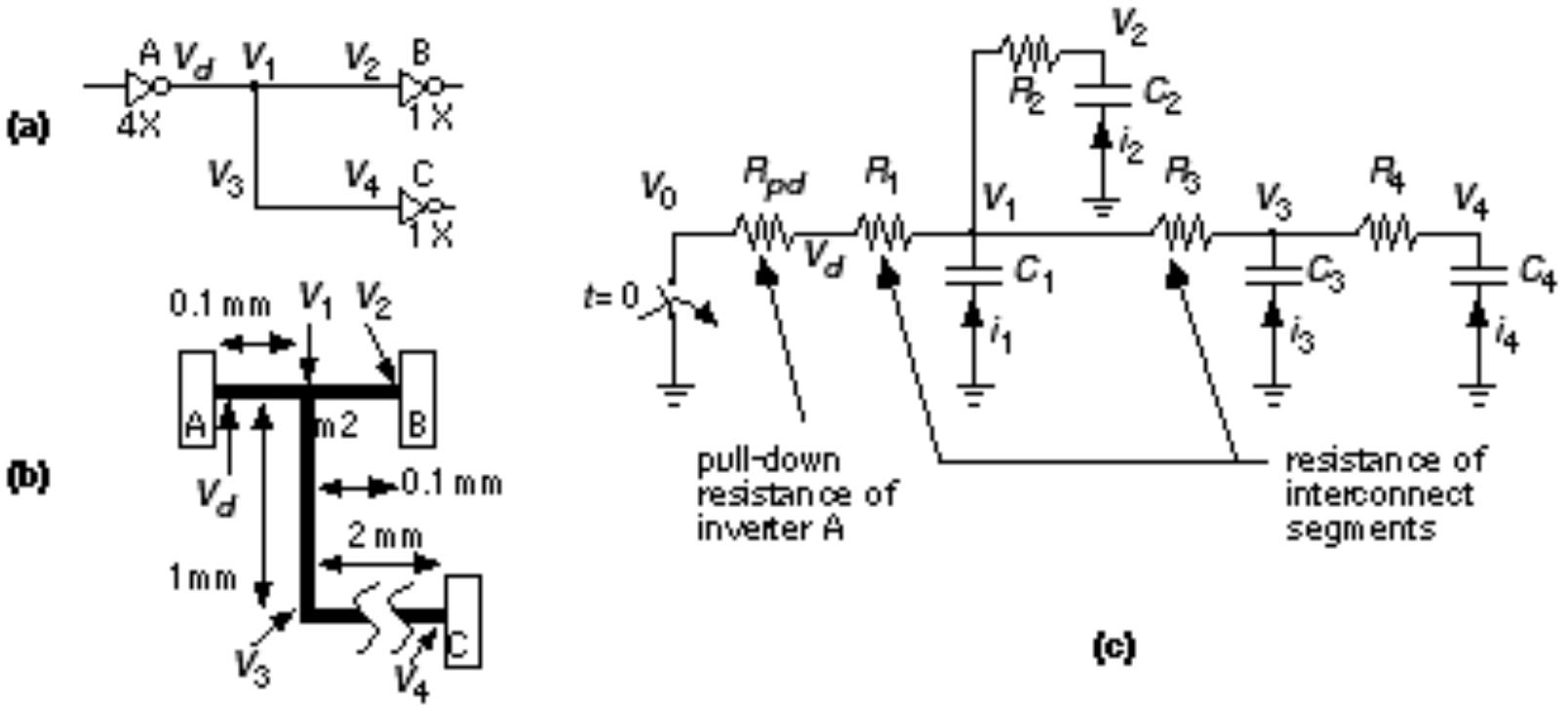


Global Routing

- Two types of areas to global route
  - inside the flexible blocks
  - between blocks
- Objectives
  - start from a floorplan and placement
  - minimize the total interconnect length
  - maximize the probability that the detailed router can complete the routing
  - minimize the critical path delay

Measurement of Interconnect Delay

- Elmore delay model
  - after placement, the logic cell position fixed

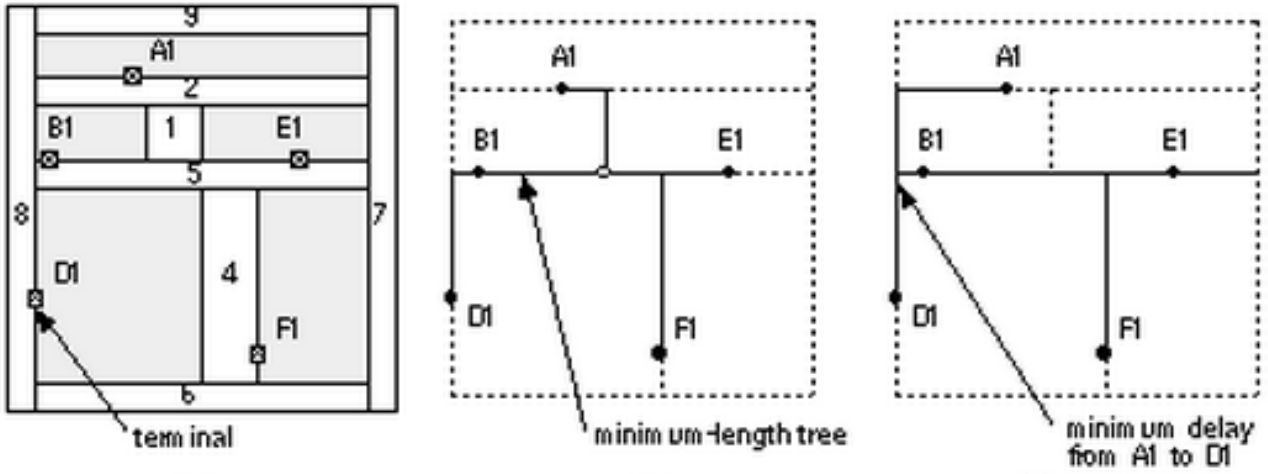


Global Routing Between Blocks

- Numbering channels
- Channels form the edge of a graph
- Each channel has a capacity

Global Routing Between Blocks

- Find terminals of nets
- Find minimum-length tree
- Minimum-length tree != Minimized delay between terminals (A1 to D1)

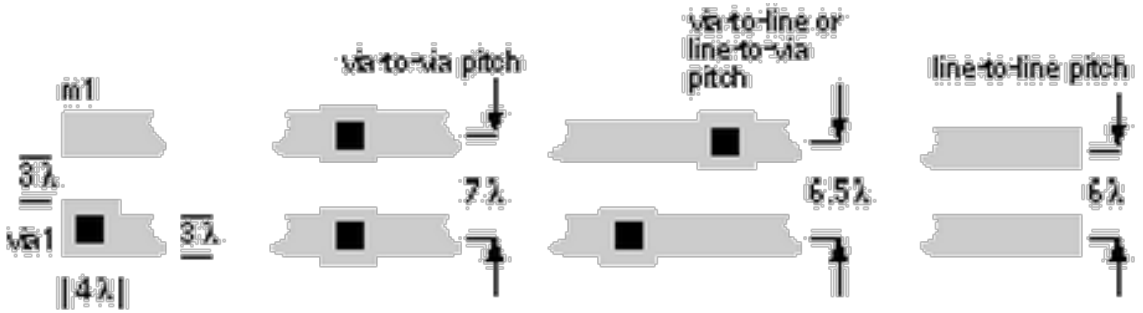


Detailed Routing

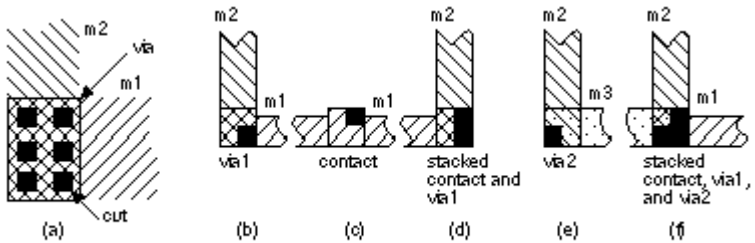
- Goal
  - complete all connections between logic cells
- Objectives
  - minimize total interconnect length and area
  - minimize # of layer changes (vias)
  - minimize delay of critical paths

Detailed Routing

- Routing pitch rules
  - via-to-via (VTV) pitch
  - via-to-line (VTL) pitch
  - line-to-line (LTL) pitch

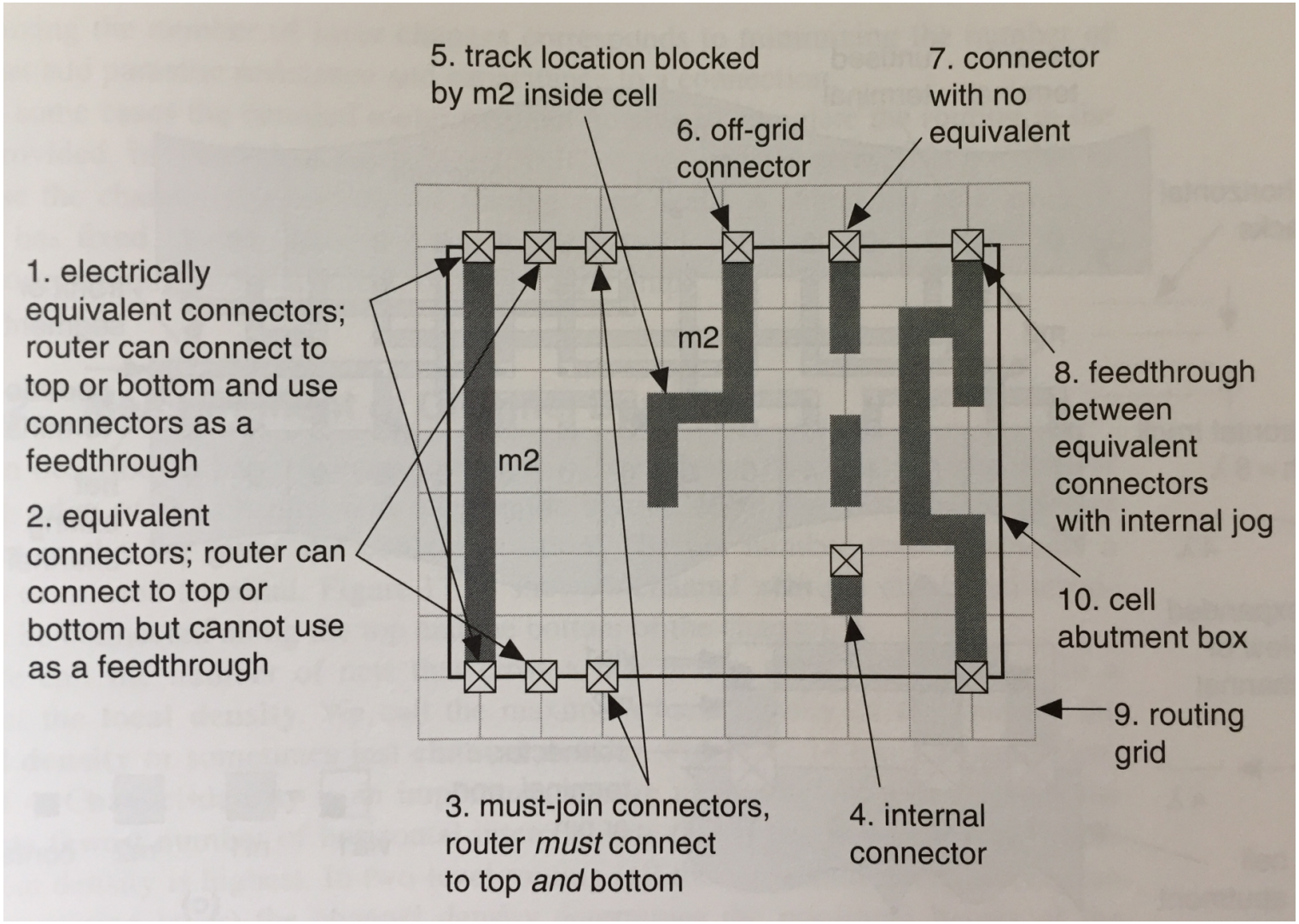


- Waffle via
- Stacked via



Router's View of the Cell

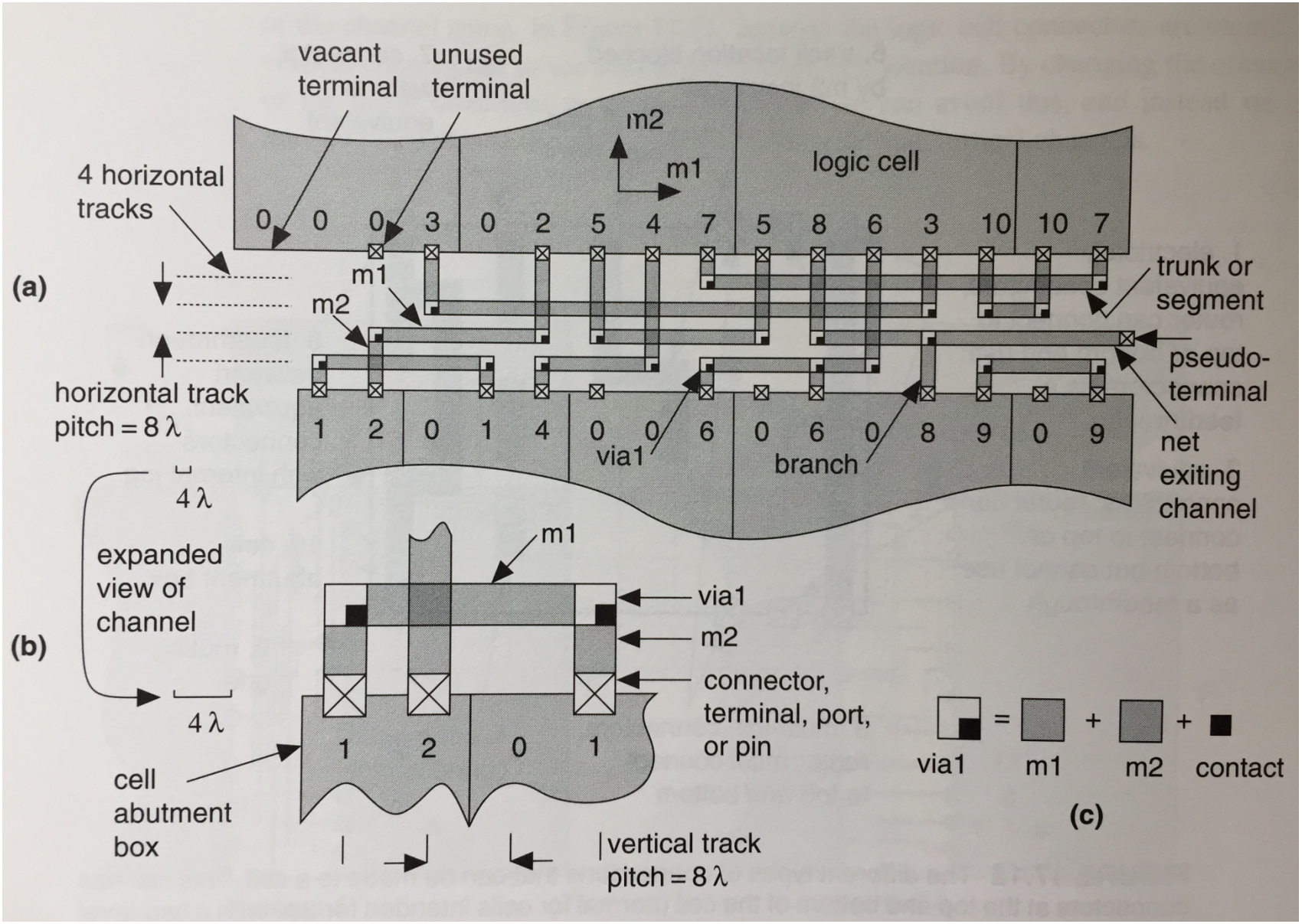
- Phantom



Terms in Detailed Routing

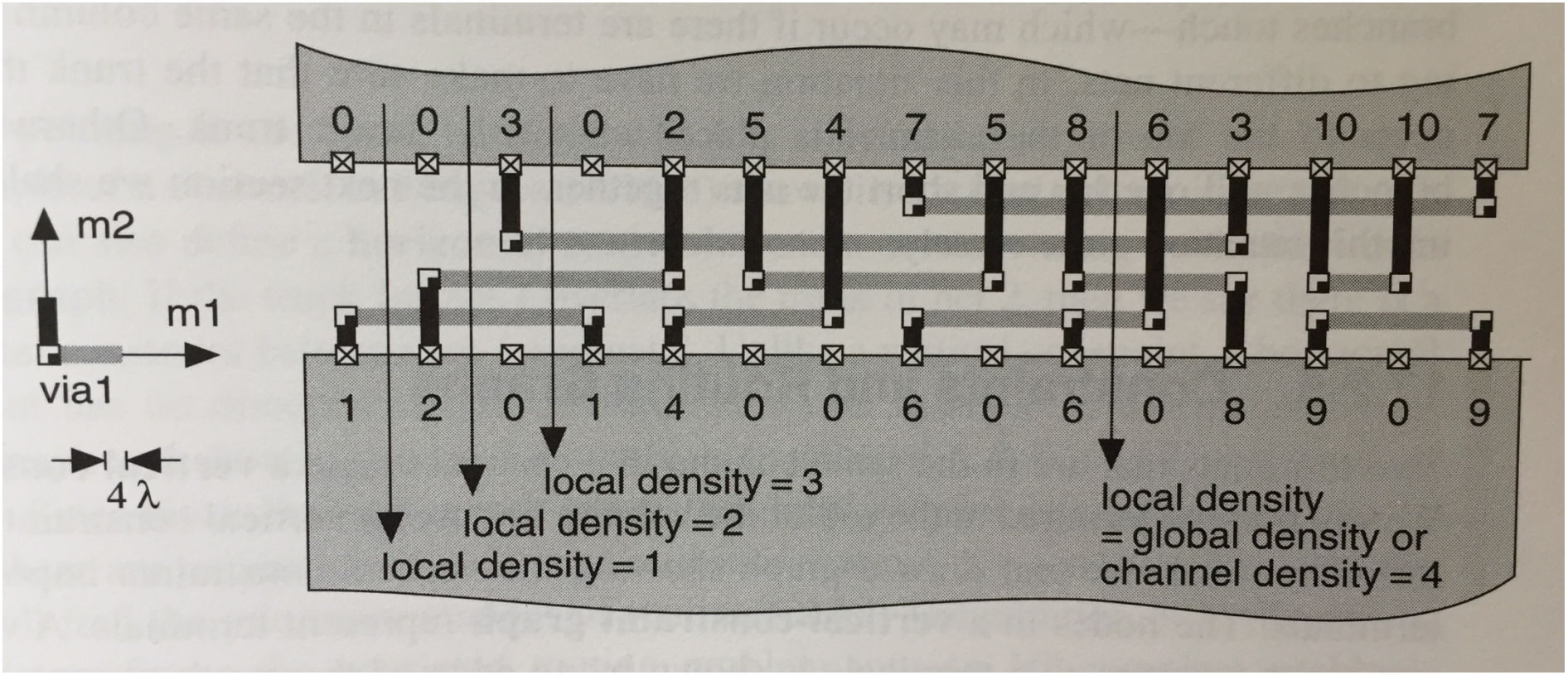
- Trunks
  - running in parallel to the channel
- Branches
  - connecting trunk to terminals
- Tracks
  - horizontal track spacing
- Terminal
  - column spacing

Terms in Detailed Routing



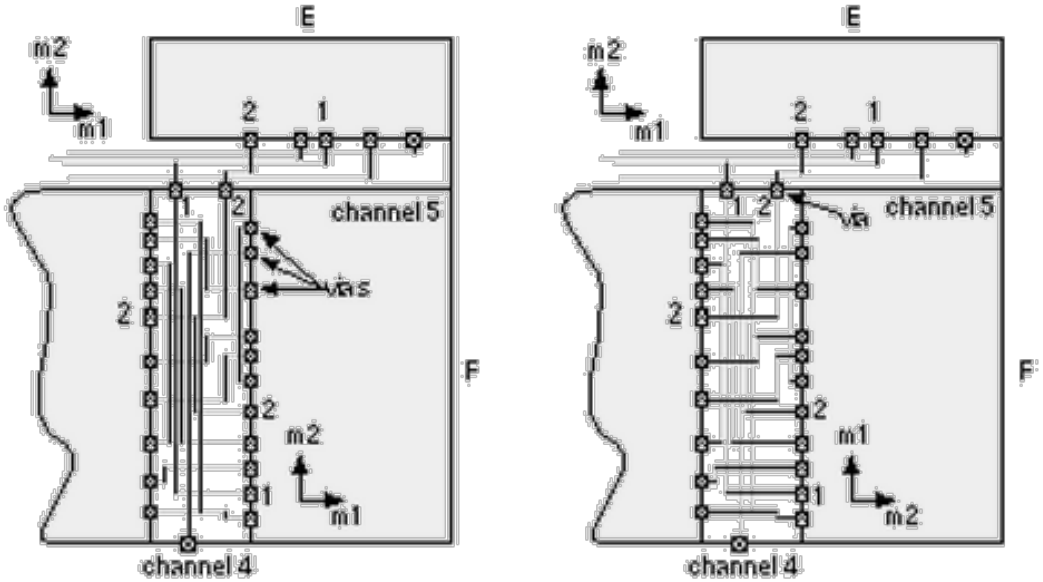
Channel Density

- Global density
- Local density



Detailed Routing

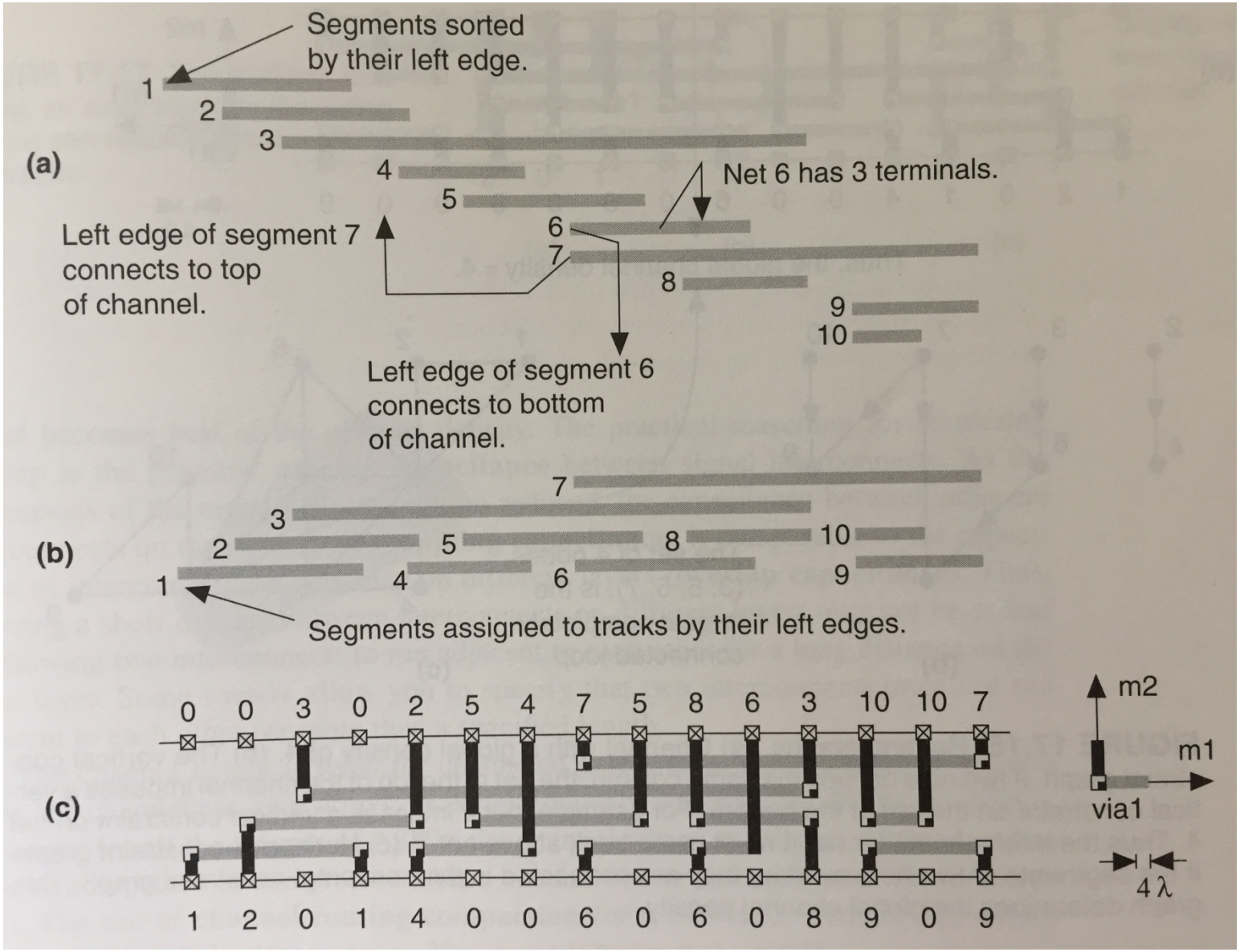
- Manhattan routing
  - preferred direction
  - preferred metal layer
  - logic cell connectors on 1 metal only



2-Layer Routing

- Left-edge algorithm
  - 1. sort the nets from the leftmost edge
  - 2. assign first net to the first free track
  - 3. assign next net that can fit to the track
  - 4. repeat step 3 until no more net can fit
  - 5. repeat step 2-4 until all nets assigned

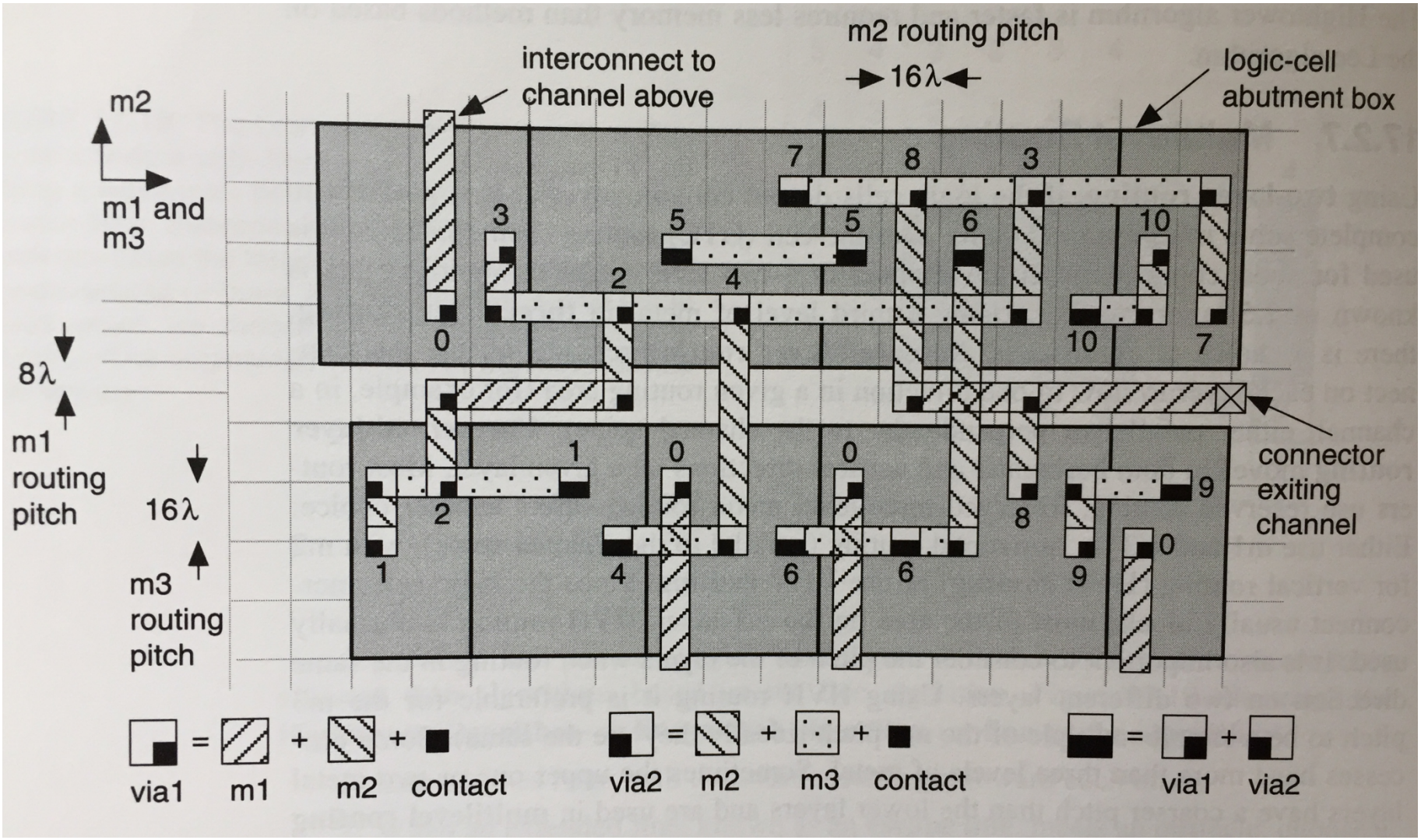
Left-Edge Algorithm Example



Multi-Layer Routing

- Polysilicon + 2-level metal
  - 2.5-layer routing
  - poly only for short connections
- 3-layer routing
  - M1 horizontal, M2 vertical, M3 horizontal (HVH)
  - M1 vertical, M2 horizontal, M3 vertical (VHV)
  - M3 pitch is multiples of M1

3-Layer Routing Example

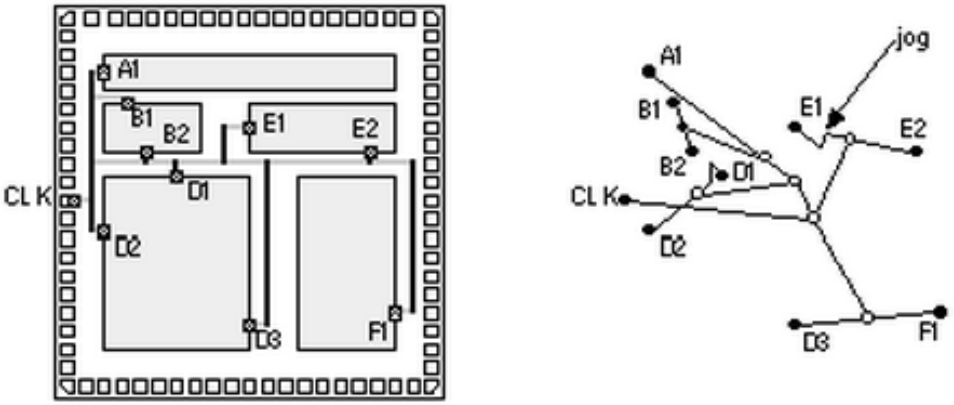


Final Routing Steps

- Timing-driven detailed routing
  - reduce # of vias
  - alter interconnect width
  - minimize overlap capacitance
- Unroutes
  - leave problematic nets unconnected
  - complete interconnects with violation
- To resolve
  - discover the reason and revisit synthesis and floorplan
  - return to global router, change bin size
  - engineering change orders (ECO)
  - via removal and routing compaction

Special Routing

- Clock Routing
  - minimize clock skew
  - clock tree synthesis
  - clock-buffer insertion



- Activity-induced skew
  - supply noise

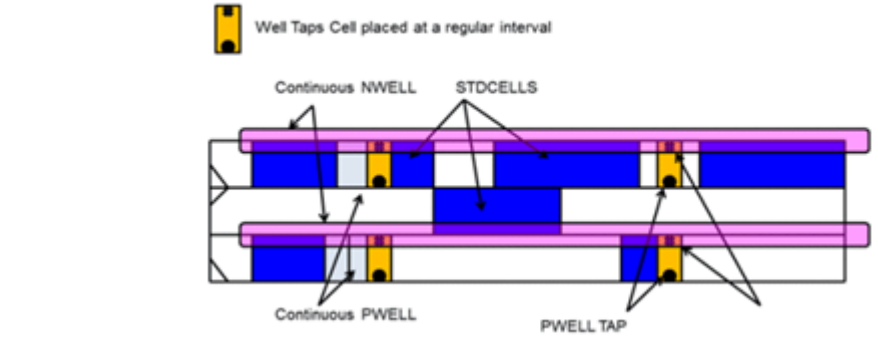
Special Routing

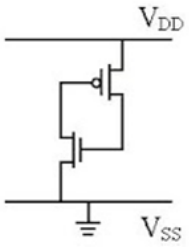
- Power Routing
  - electromigration
  - size the power buses according to the current

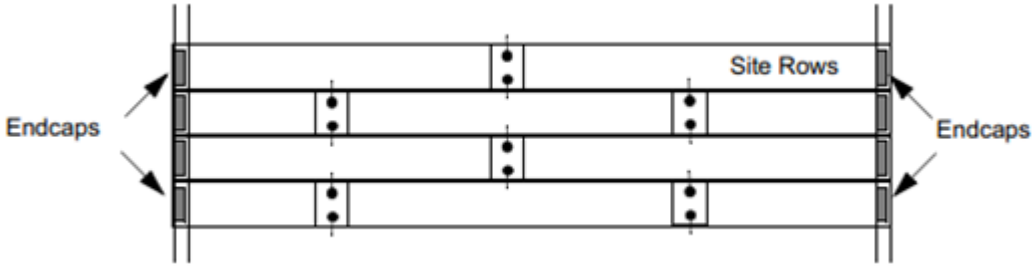
TABLE 17.1 Metallization reliability rules for a typical 0.5 micron (l = 0.25 m m) CMOS process.

Layer/contact/via	Current limit [1]	Metal thickness [2]	Resistance [3]
m1	1 mA m m $^{-1}$	7000 Å	95 m W /square
m2	1 mA m m $^{-1}$	7000 Å	95 m W /square
m3	2 mA m m $^{-1}$	12,000 Å	48 m W /square

  - tap-cell
  - end-cap cell
  - de-cap cell







Notes

- Encounter tutorial to be discuss next lecture
- Detailed class project description
  - to be release by Friday
  - behavioral code to be submitted
  - account for 30% of the project
  - by 11/22 before thanksgiving
  - if late, by 11/28, discount by 40%

Questions?

Comments?

Discussion?