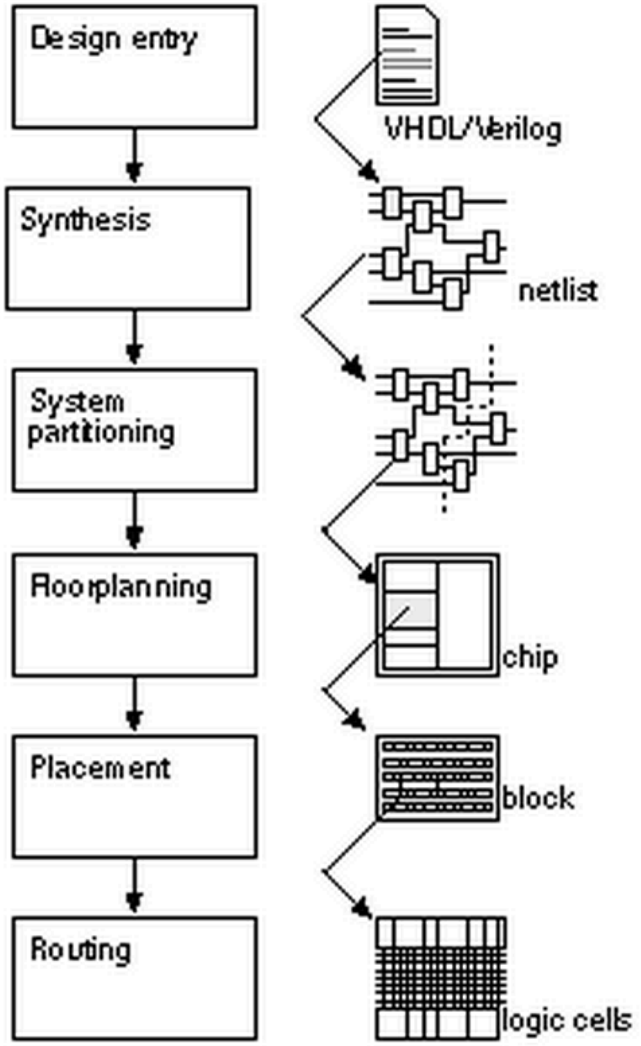
Lecture 15
Physical Design, Part 1

Xuan ‘Silvia’ Zhang
Washington University in St. Louis

http://classes.engineering.wustl.edu/ese461/

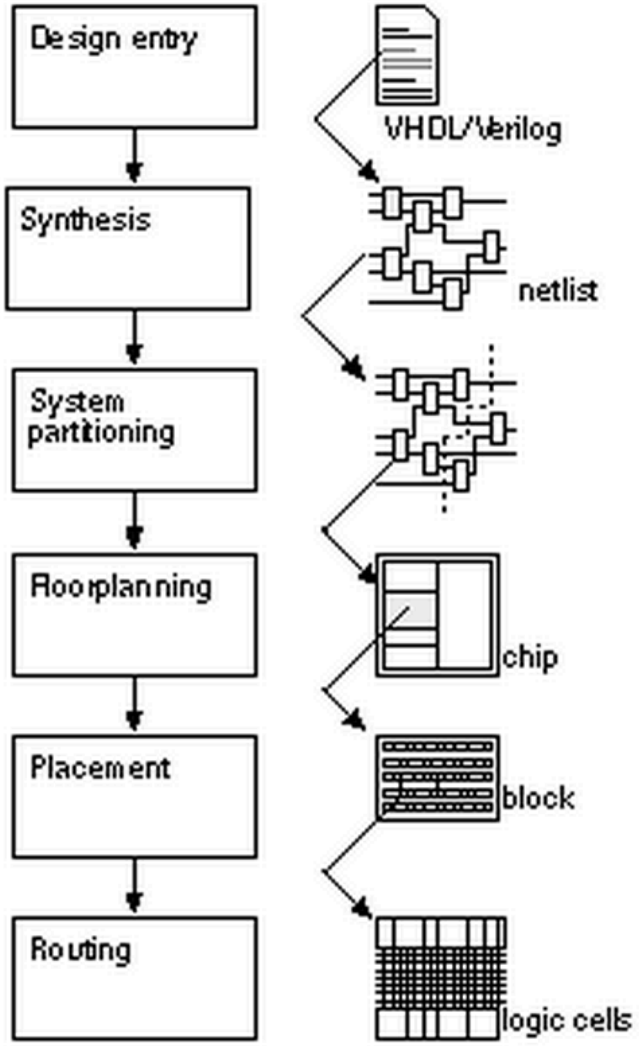
ASIC Construction

- System partitioning
  - goal: partition a system into a number of modules
  - objectives: minimize the number of external connections; keep each module smaller than max size
- Floorplanning
  - goal: calculate the sizes of all the blocks and assign them locations
  - objectives: keep the highly connected blocks physically close to each other



ASIC Construction

- Placement
  - goal: assign the interconnect areas and the location of all the logic cells within the flexible blocks
  - objectives: minimize the area and the interconnect density
- Global routing
  - goal: determine the location of all the interconnect
  - objective: minimize total interconnect area
- Detailed routing
  - goal: completely route the chip
  - objective: minimize total length of the interconnect

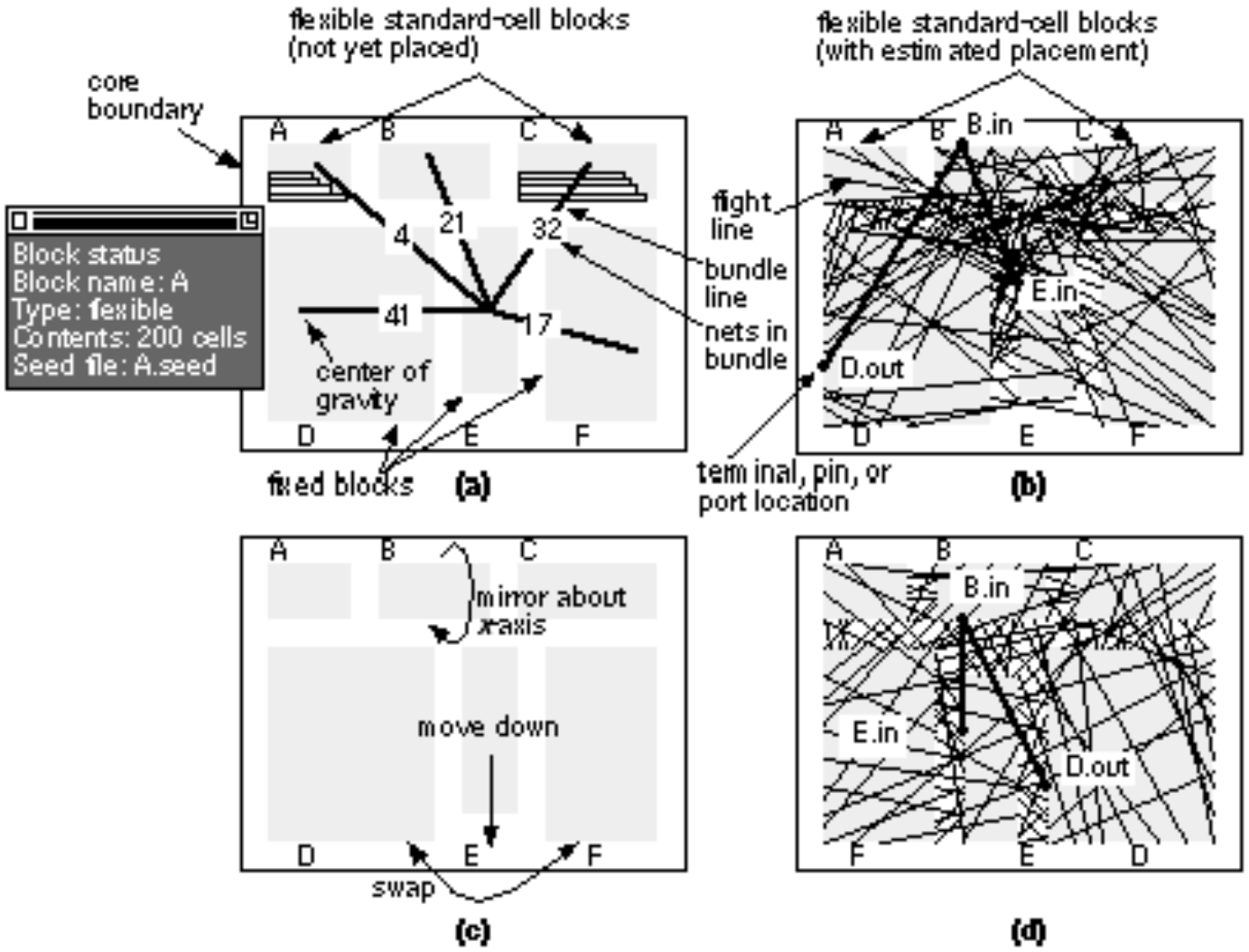


Floorplanning

- Mapping between logical and physical design
  - interconnect delay dominates gate delay
  - center of ASIC backend design operation
  - timing-driven floorplanning
- Goals
  - arrange the blocks on a chip
  - decide the location of the I/O pads
  - decide the location and number of the power pads
  - decide the location and type of clock distribution
- Objectives
  - minimize chip area and delay
  - how to measure?

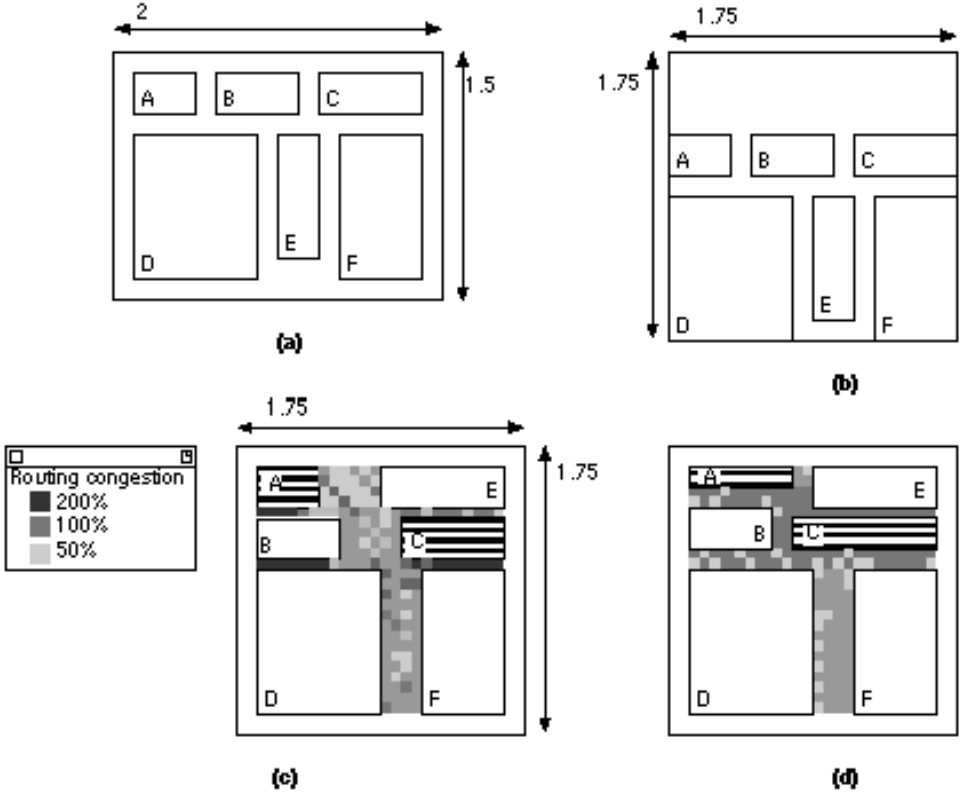
Floorplanning

- Relative position, orientation



Floorplanning

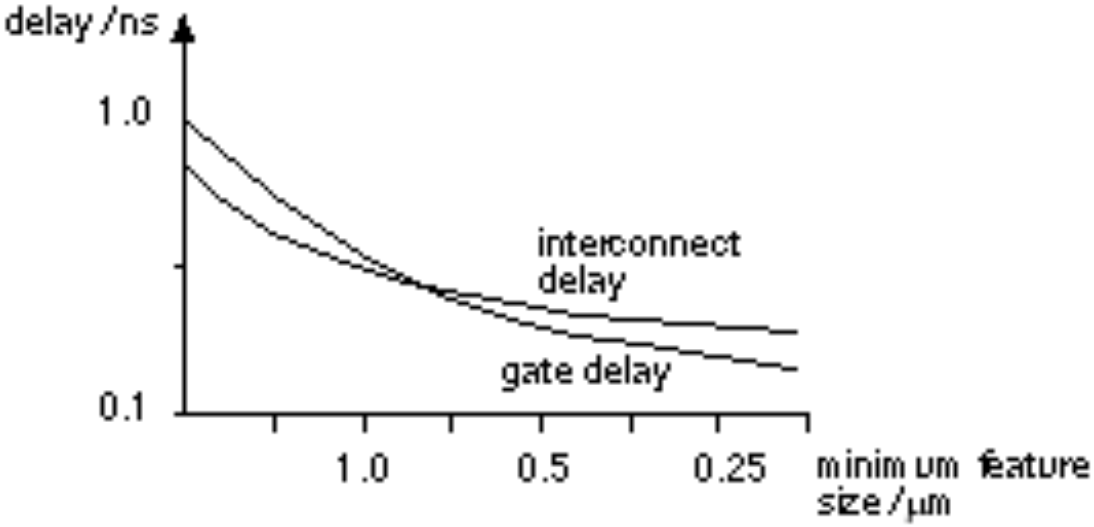
- Aspect ratio



- Initial seeding
  - hard seed, soft seed

Measurement of Delay

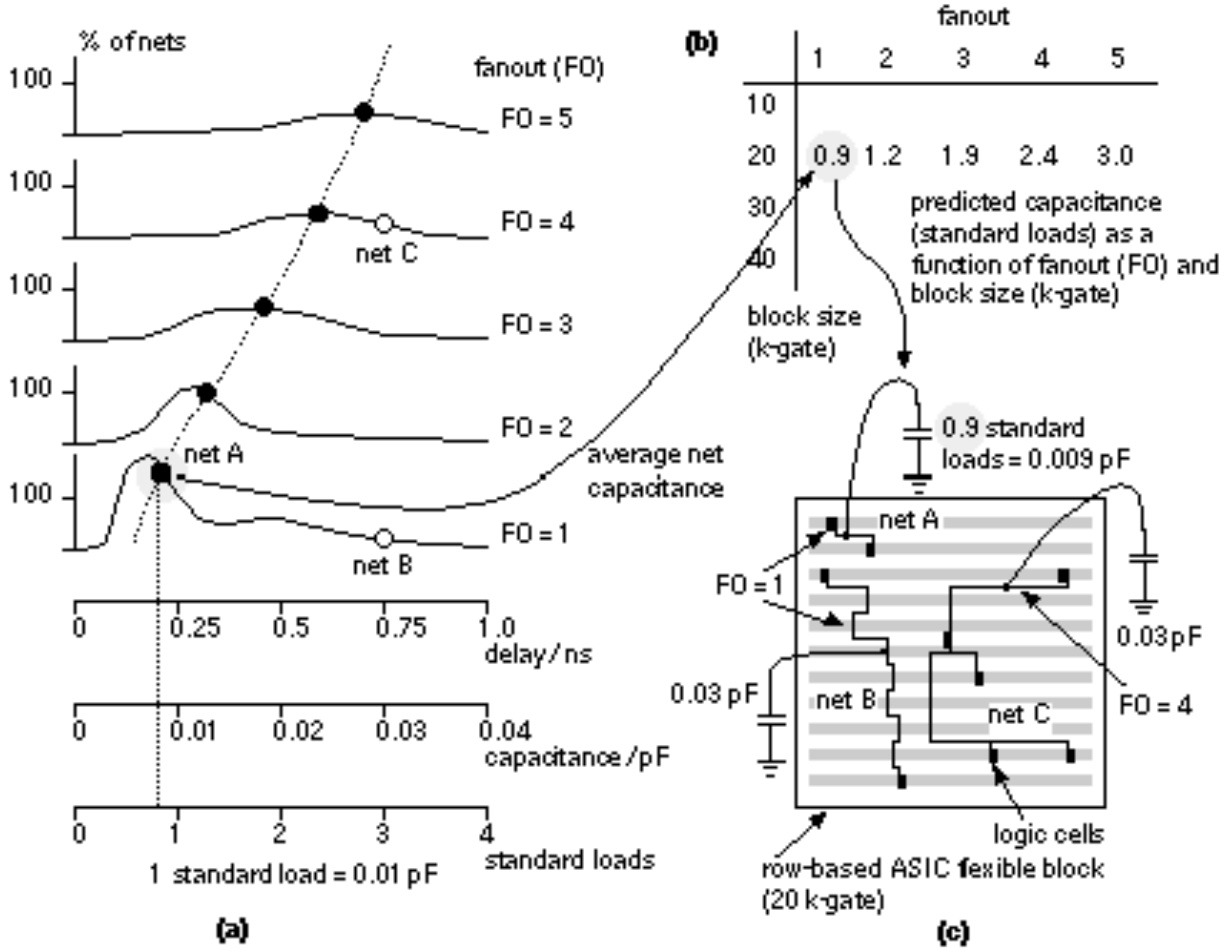
- Gate delay vs interconnect delay



- Predict interconnect delay
  - does not know interconnect capacitance or resistance
  - have to infer based on fanout (FO)

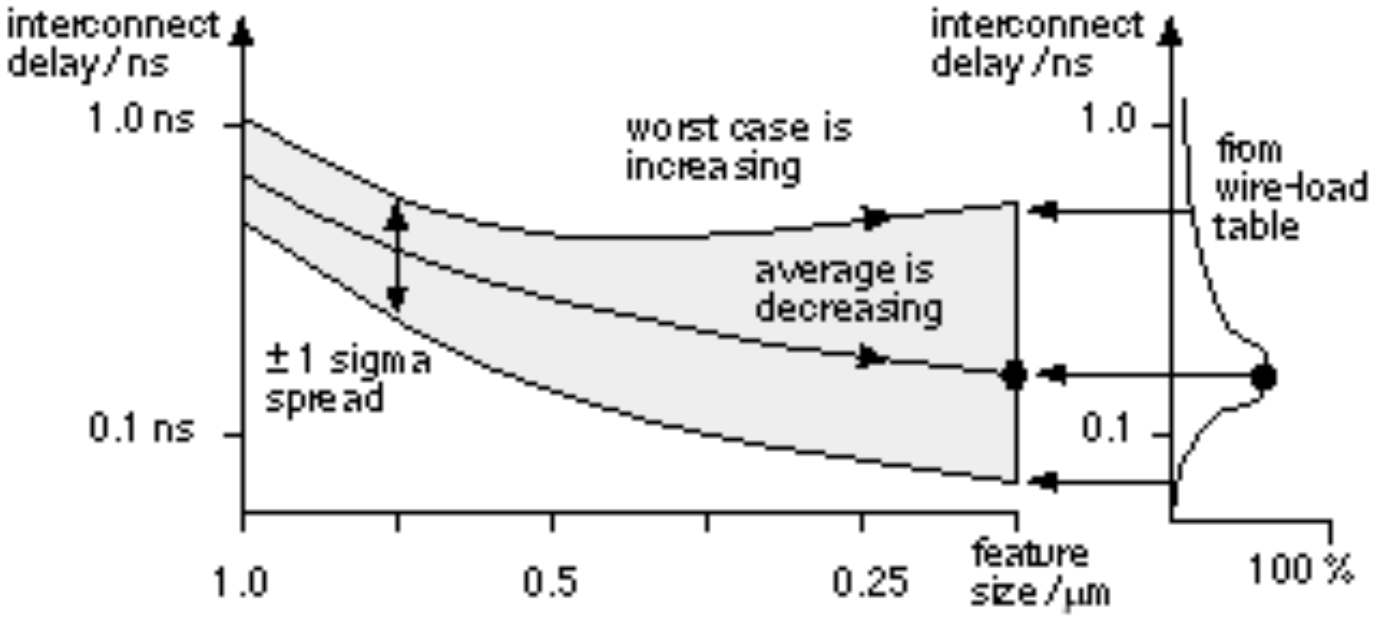
Predicted-Capacitance Tables

- Predict capacitance with FO and logic size



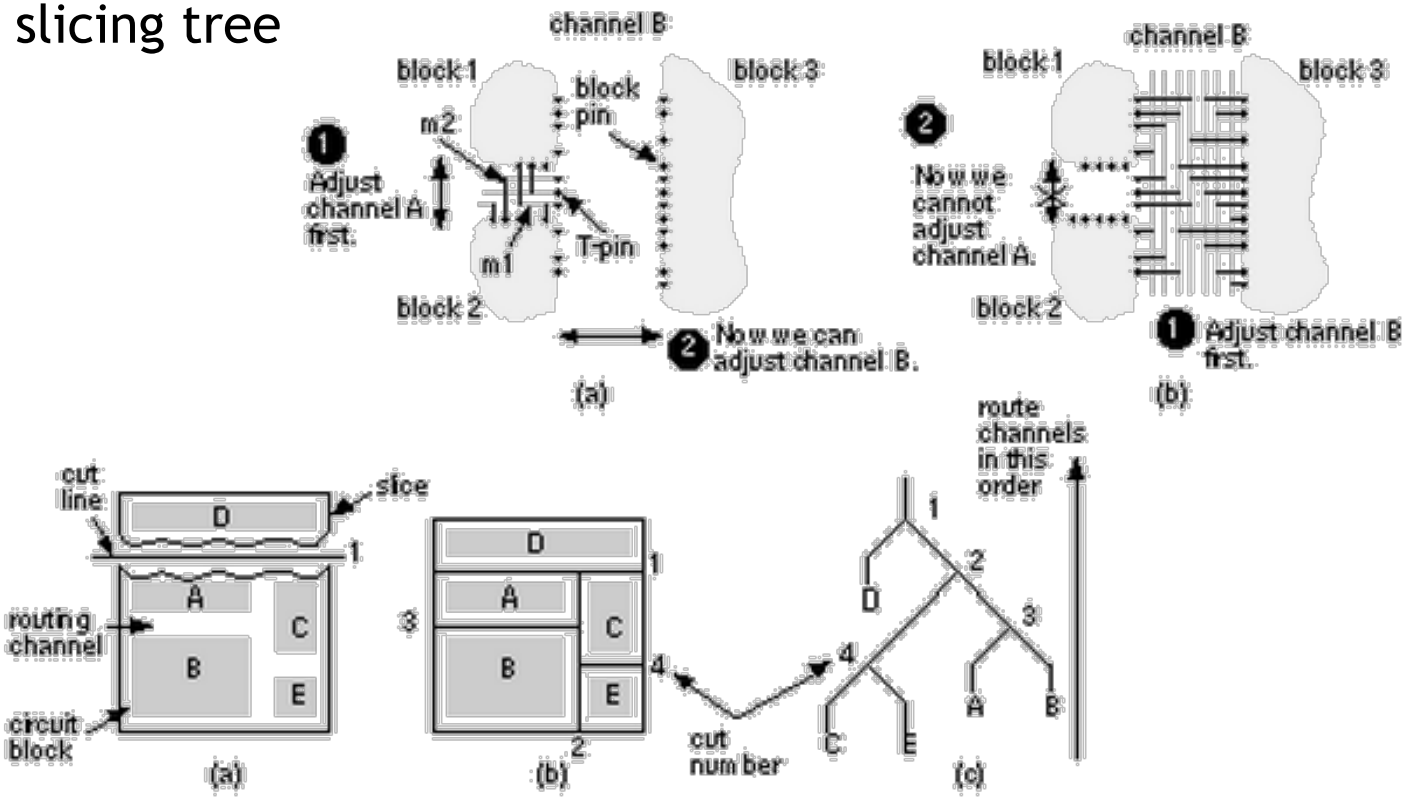
Worst-Case Interconnect Delay

- Interconnect delay trends
  - fixed chip size
  - coast-to-coast interconnect
  - increased worst-case delay at smaller technology nodes



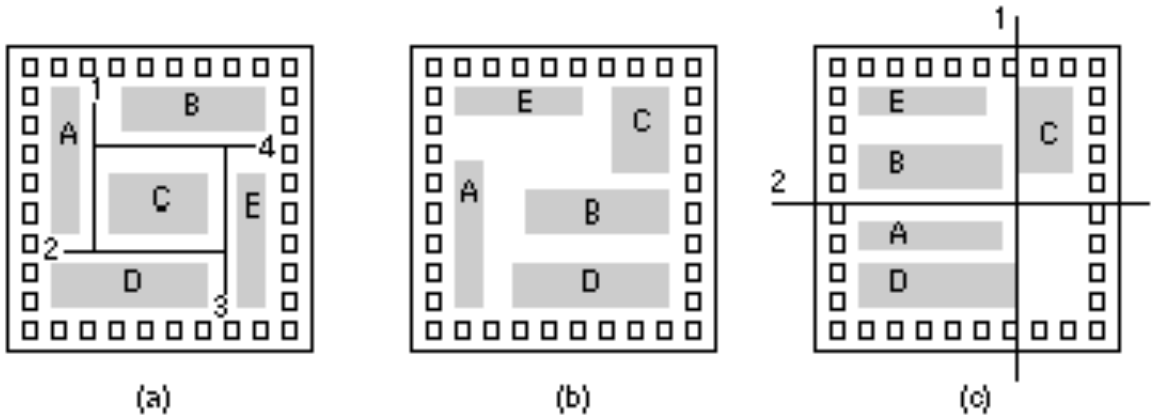
Channel Definition

- Assign the areas between blocks for interconnect
- Channel ordering
  - stem first, bar second
  - slicing floorplan (T junction)
  - slicing tree

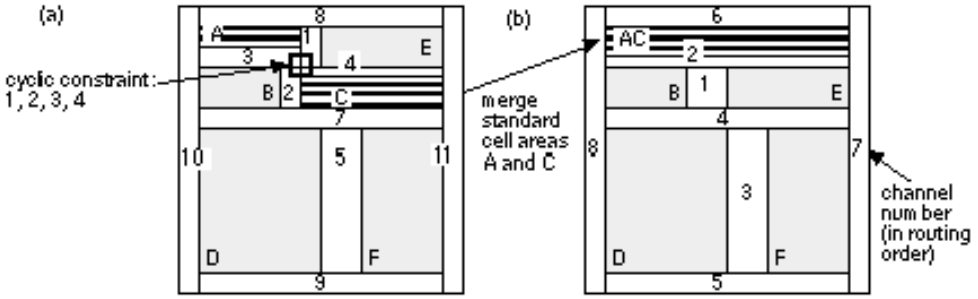


Cyclic Constraints

- No slicing the floorplan without breaking blocks

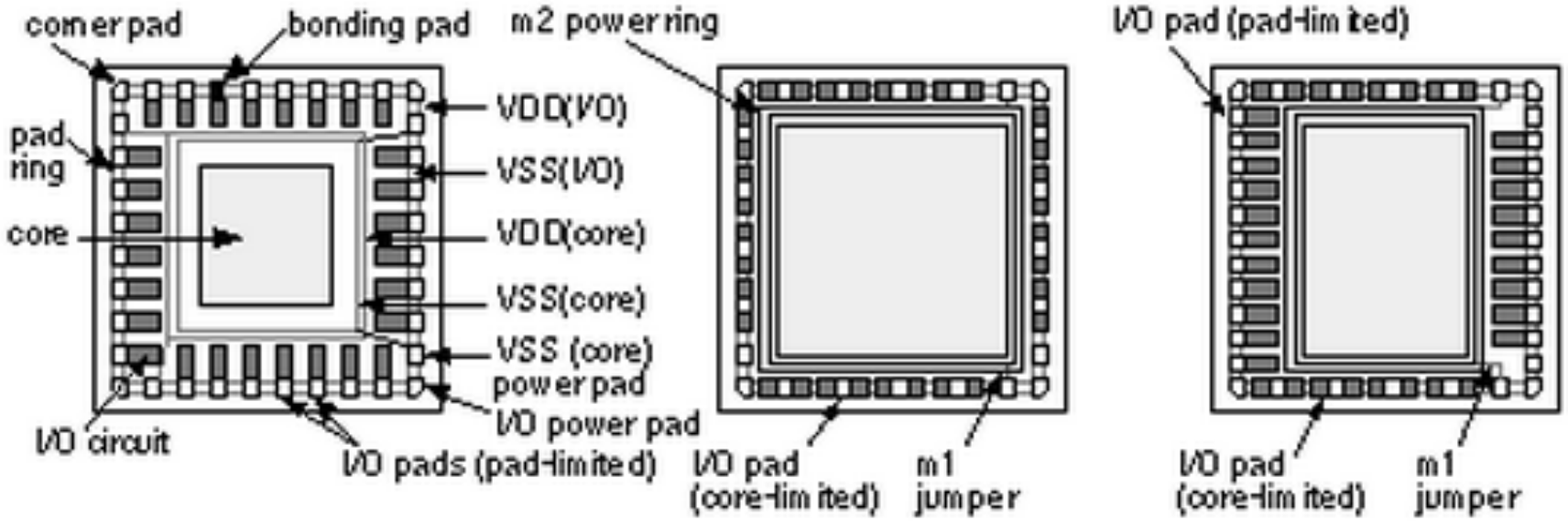


- Merge
- Selective flattening
- Routing order



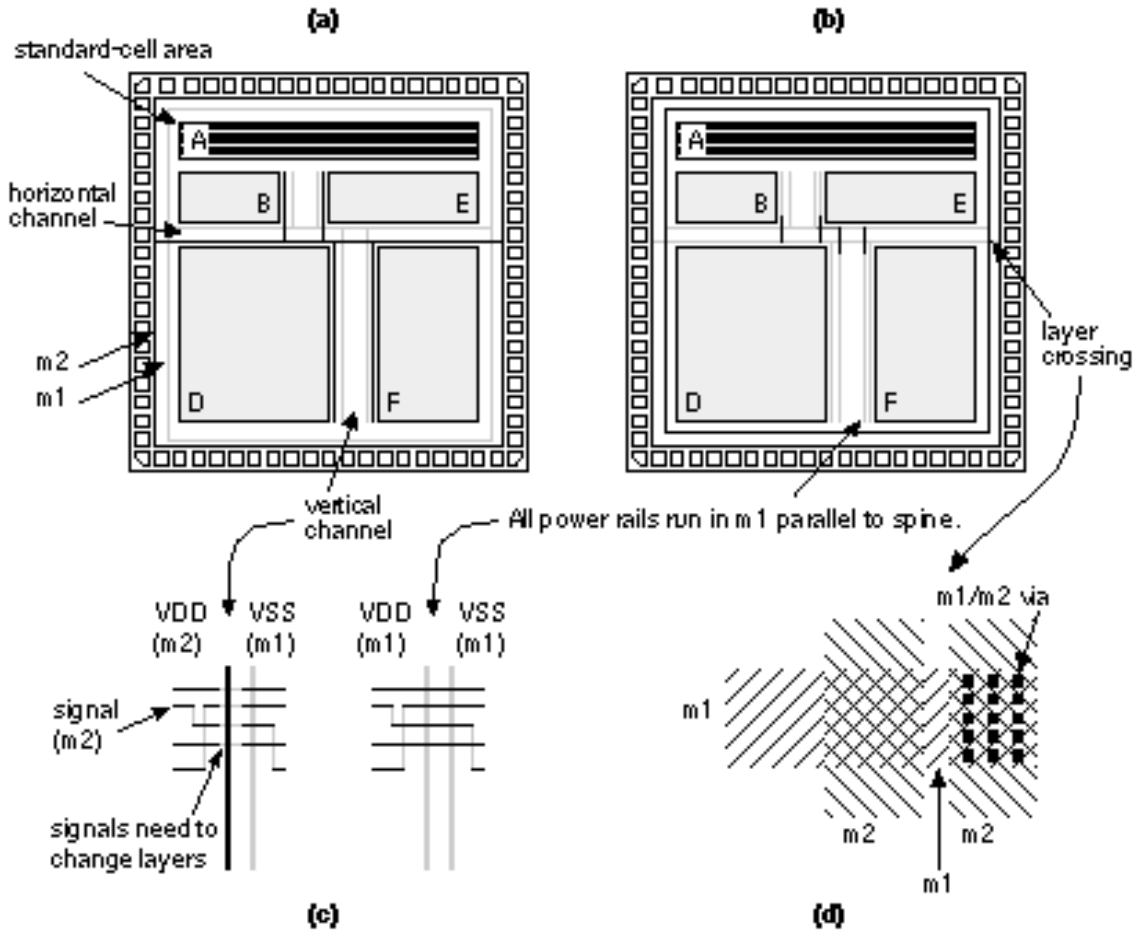
I/O Pad Planning

- Pad-limited and core-limited chip
- Pad slot and pad pitch



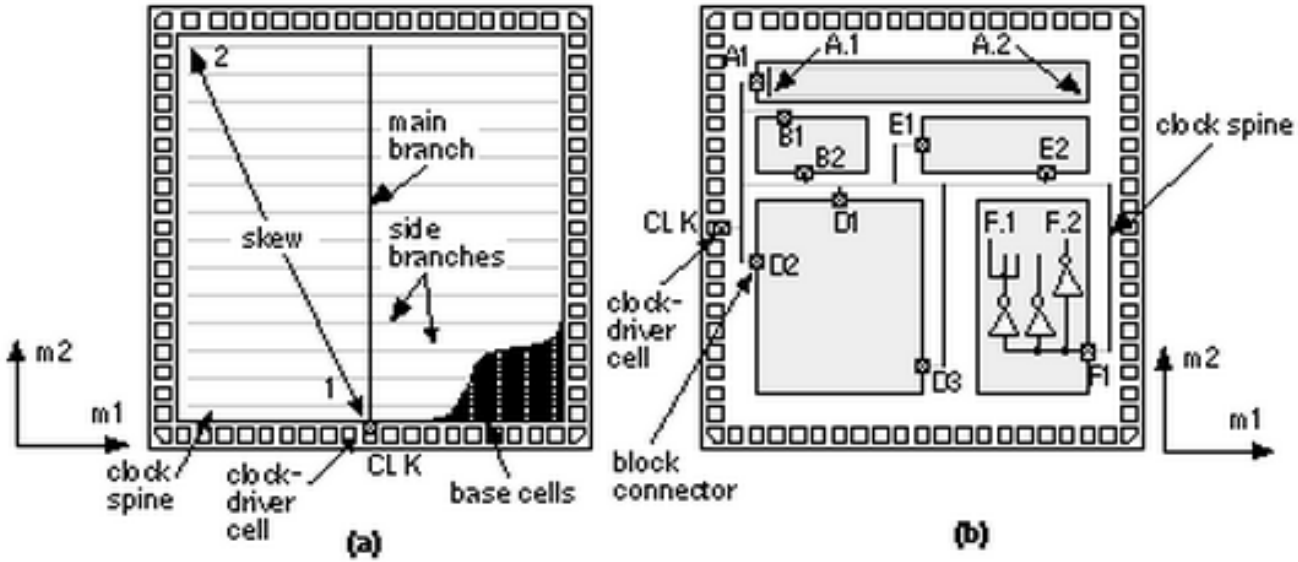
Power Planning

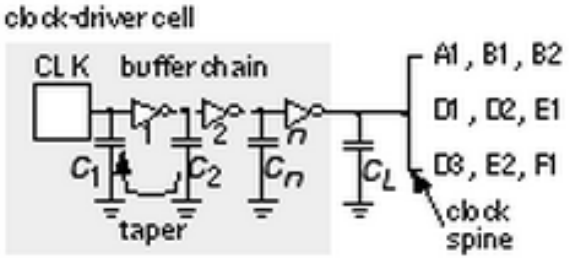
- Power distribution
- Pad slot and pad pitch

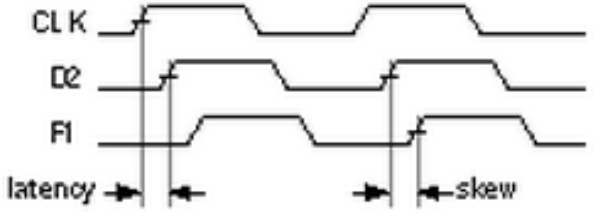


Clock Planning

- Clock spine (fish-bone clock distribution)
- Clock latency and skew
- Clock buffer

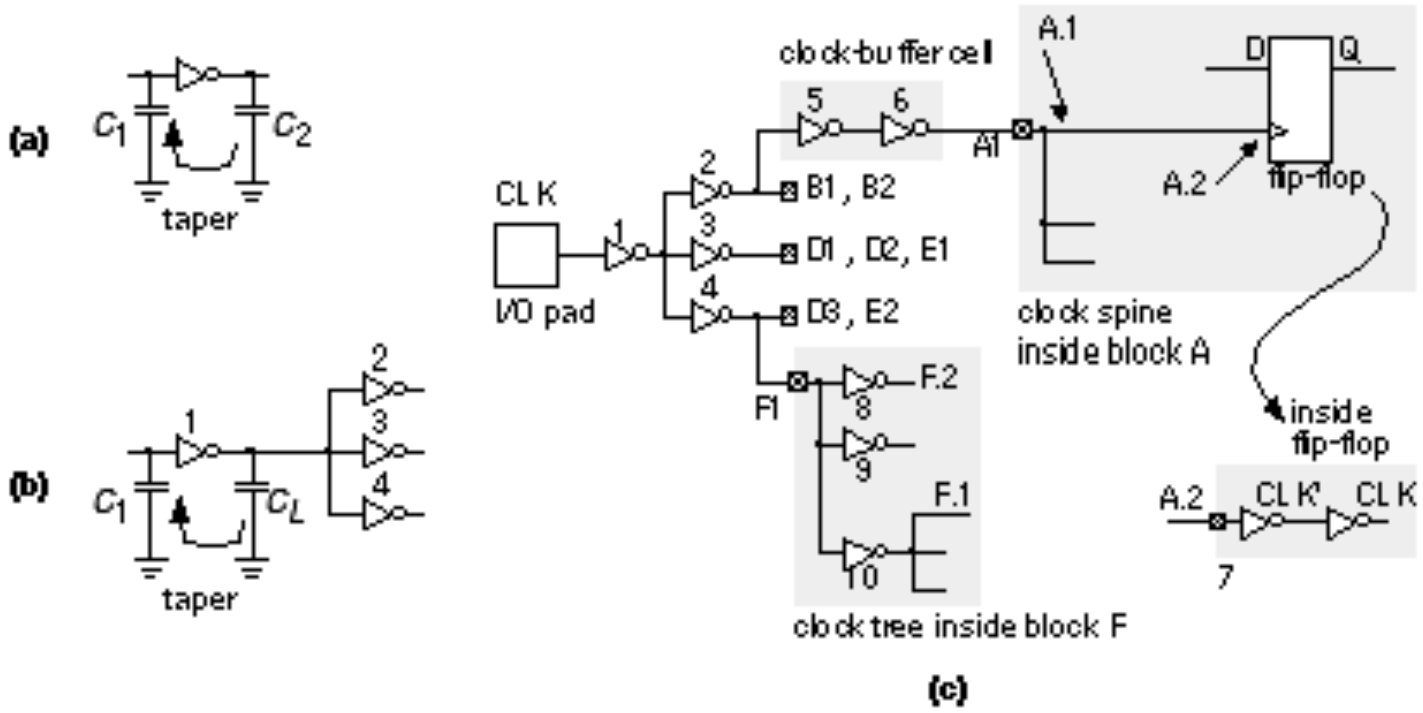






Clock Tree

- Minimum delay when taper ratio is e=2.7
- need to balance the delays through the tree



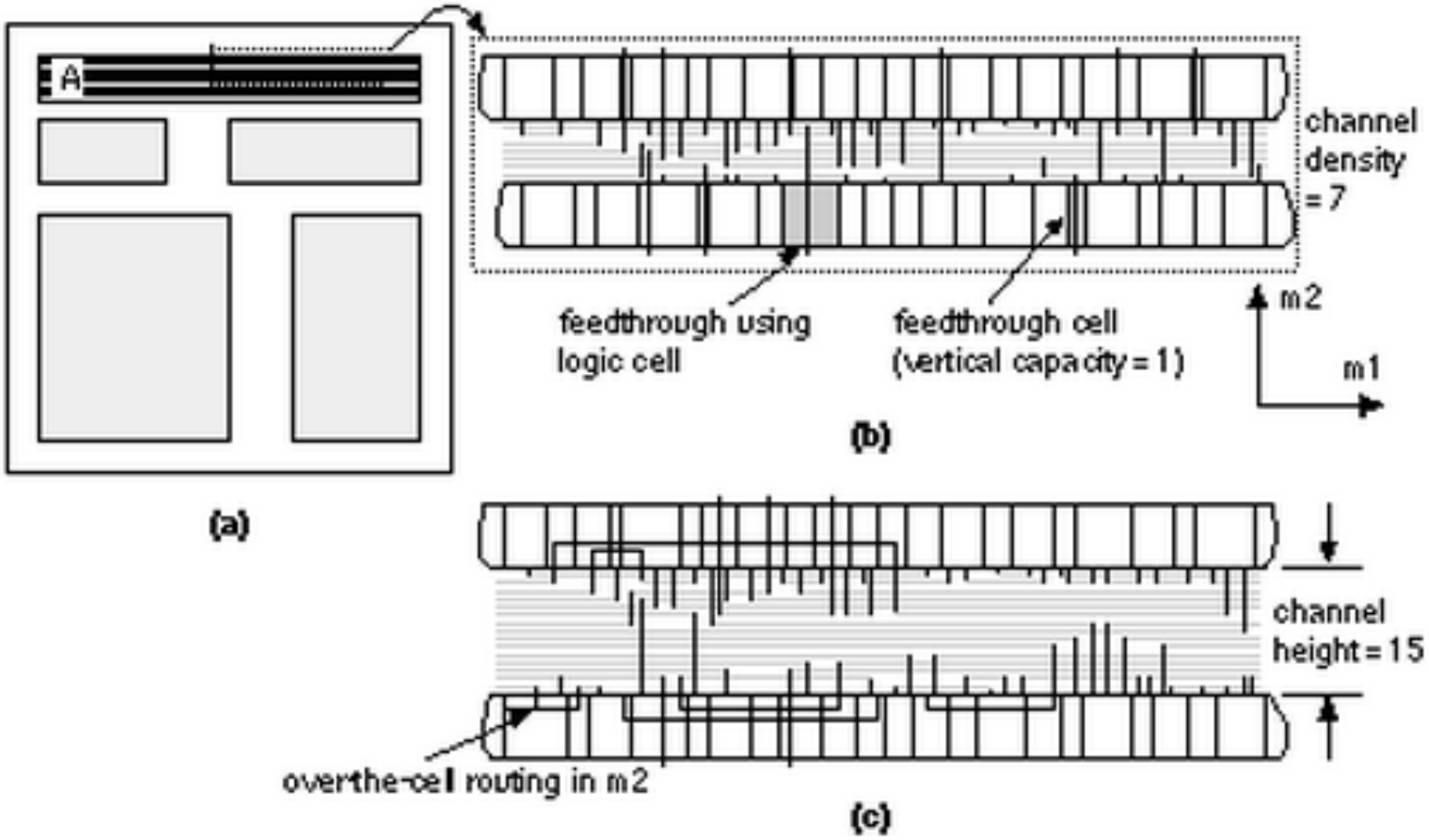
Placement

- Place logic cells within the flexible blocks
- Ideal objectives
  - guarantee the router can complete the routing step
  - minimize all the critical net delays
  - make the chip as dense as possible
  - minimize power, crosstalk between signals

- Realistic objectives
  - minimize total estimated interconnect length
  - meet the timing requirement for critical nets
  - minimize the interconnect congestion

Placement Terms

- Over the cell routing (OTC)
- Channel capacity
- Feedthroughs (feedthrus)
- Jumper (unused vertical track in a cell)



Reference

- Cadence Encounter Tutorial posed online

- ASIC ebook, Chapter 16
  - http://www10.edacafe.com/book/ASIC/Book/CH16/CH16.php

Questions?

Comments?

Discussion?

LEF and DEF Files (Cadence)

- Library exchange format (LEF)
  - Standard Cadence tools
  - Describe IC process and a logic cell library
    - gate array: cells, logic, size, connectivity
- Design exchange format (DEF)
  - Describe all physical aspects of a chip design
  - Netlist and physical location
  - Exchange information between designs