Lecture 13
Timing Analysis, Part 2

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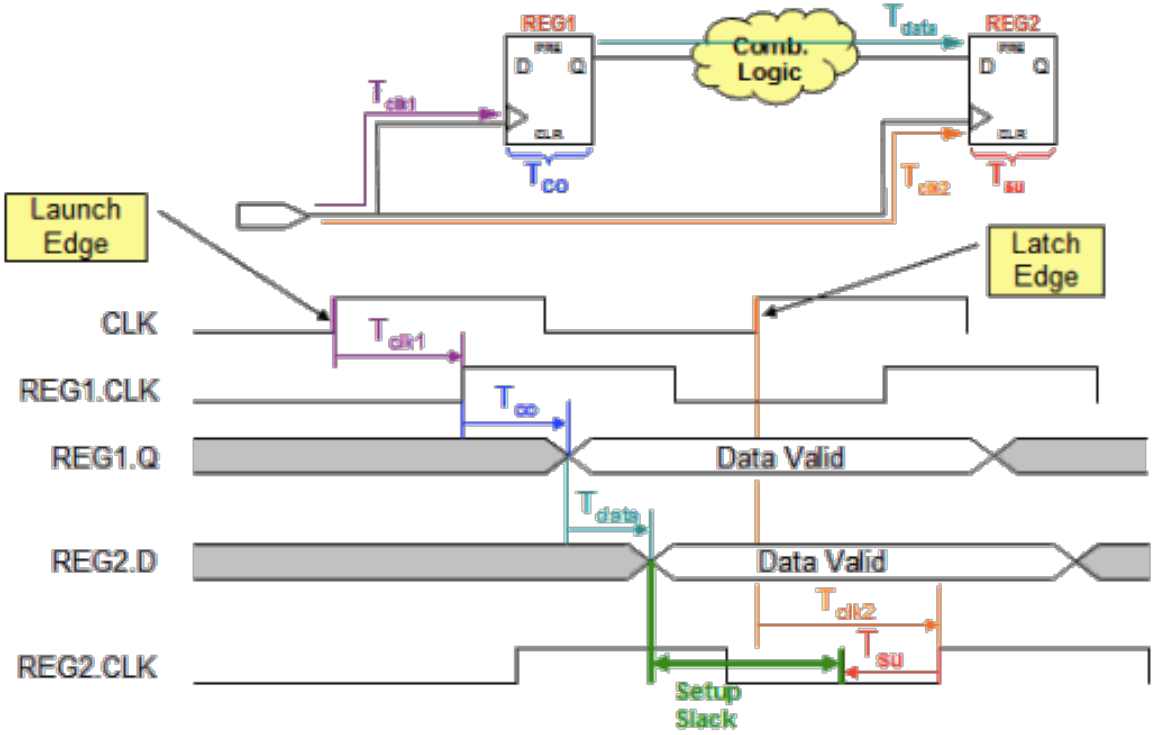
http://classes.engineering.wustl.edu/ese461/

Review: Timing in Digital Logic

- Setup slack



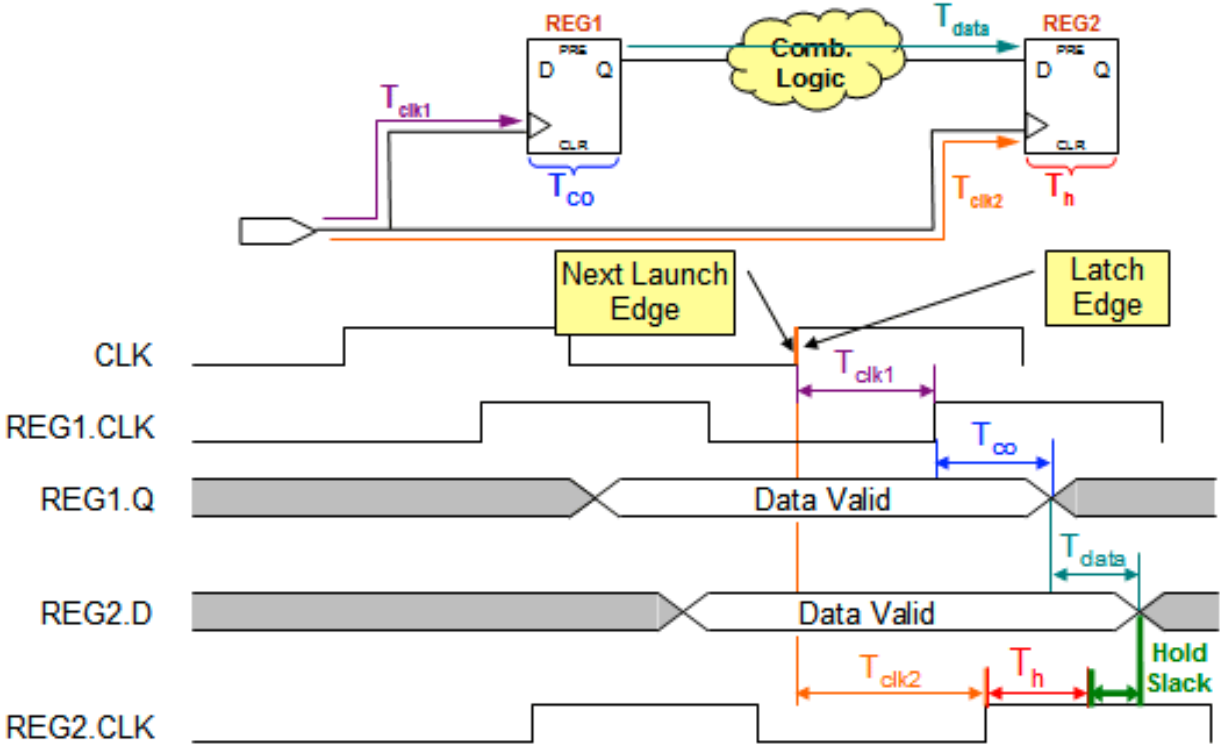
Setup Slack = Data Required Time – Data Arrival Time

Positive slack
Timing requirement me

Negative slack
Timing requirement not met

Review: Timing in Digital Logic

- Hold slack



Hold Slack = Data Arrival Time – Data Required Time

Positive slack
Timing requirement me

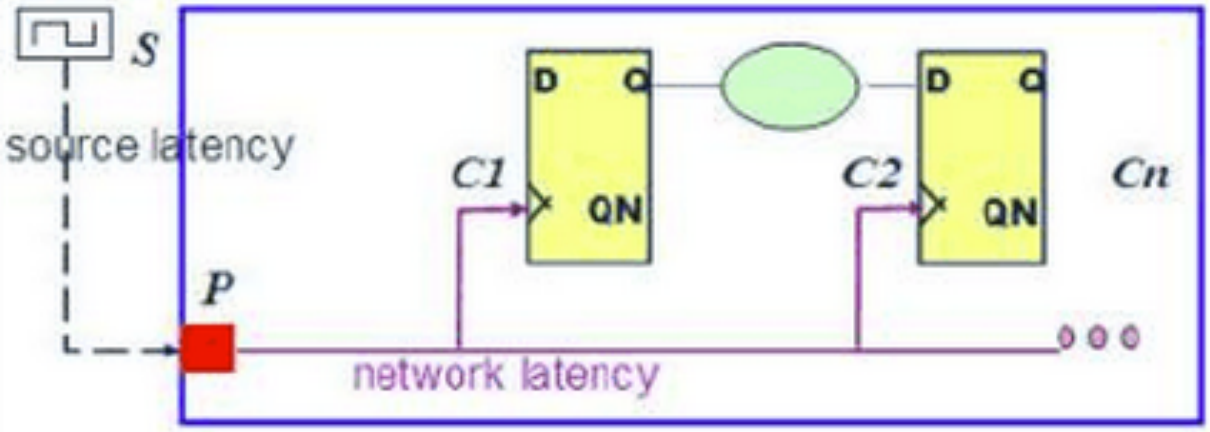
Negative slack
Timing requirement not met

Review: Static Timing Analysis

- Timing Type
  - Combinational Timing (Delay)
  - Setup Timing (Check)
  - Hold Timing (Check)
  - Edge Timing (Delay)
  - Present and Clear Timing (Delay)
  - Recovery Timing (Check)
  - Removal Timing (Check)
  - Three State Enable & Disable Timing (Delay)
  - Width Timing (Check)
- Interconnect Delay

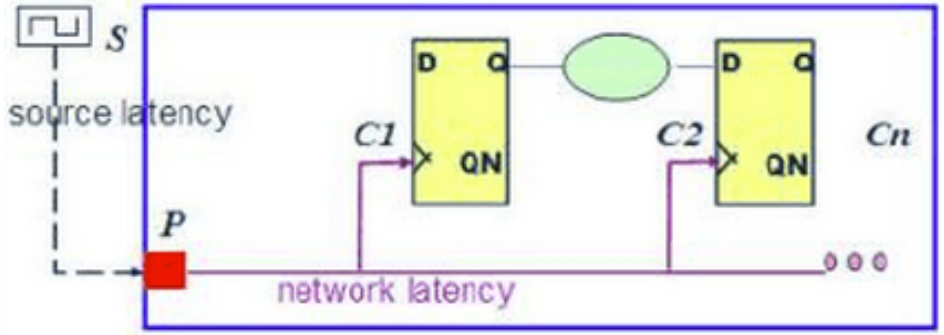
Static Timing Analysis

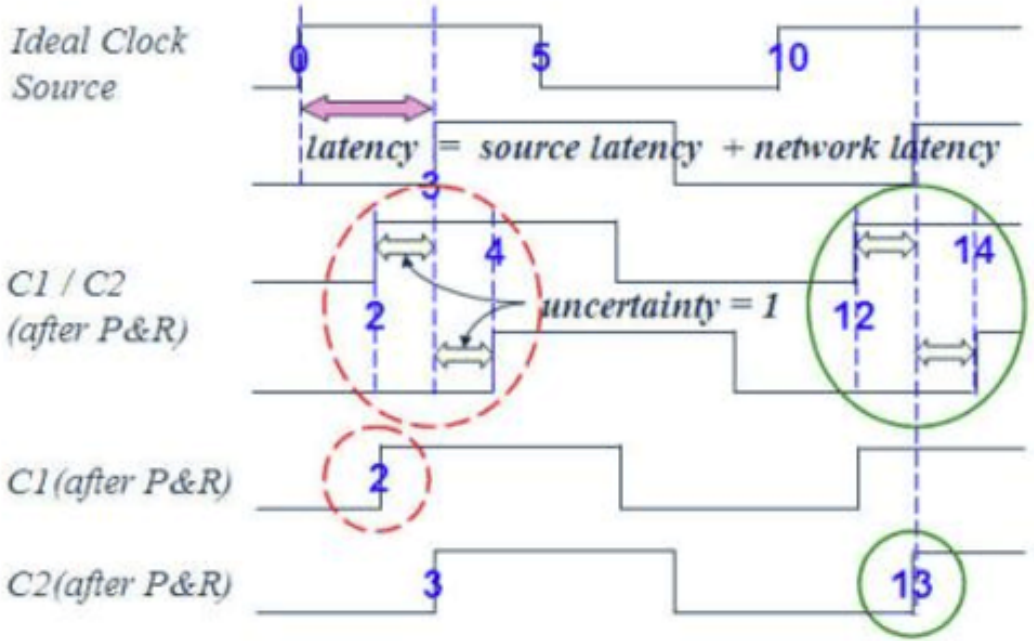
- Timing Constraints
  - path delay between two flip-flops must be less than one clock period
  - once clock specification is fixed, timing constraint is fixed between all flip flops



Static Timing Analysis

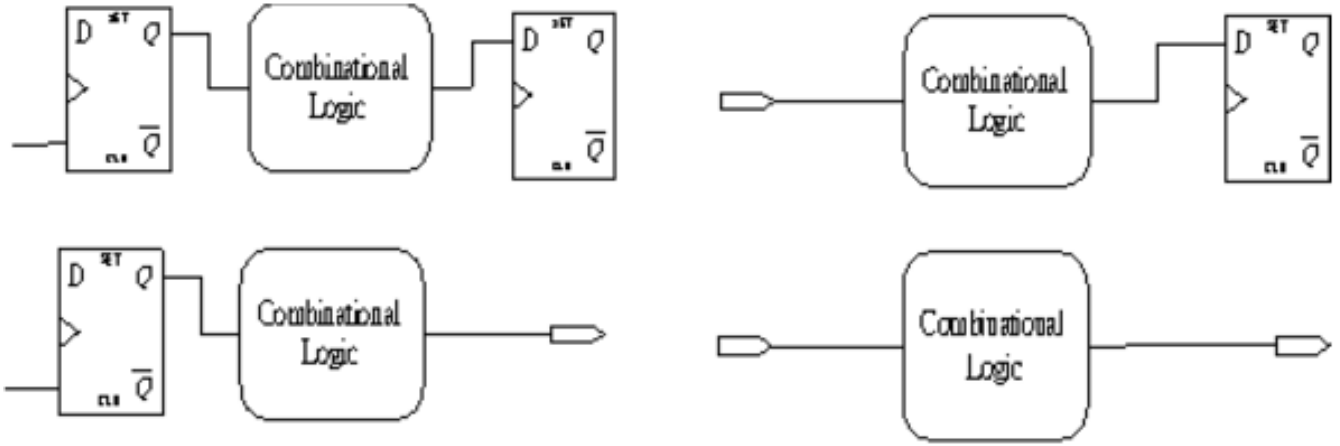
- Clock Specification
  - period
  - source latency
  - network latency
  - uncertainty
  - skew





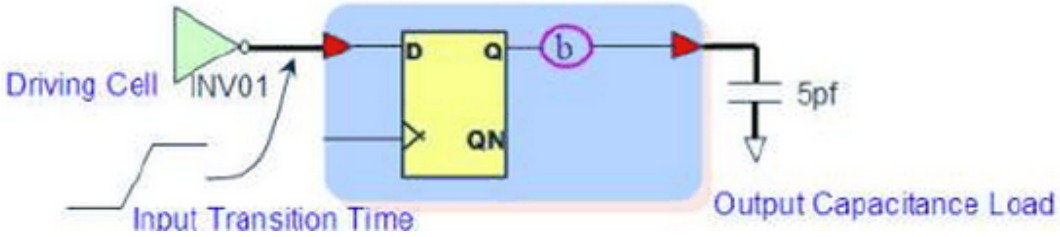
Static Timing Analysis

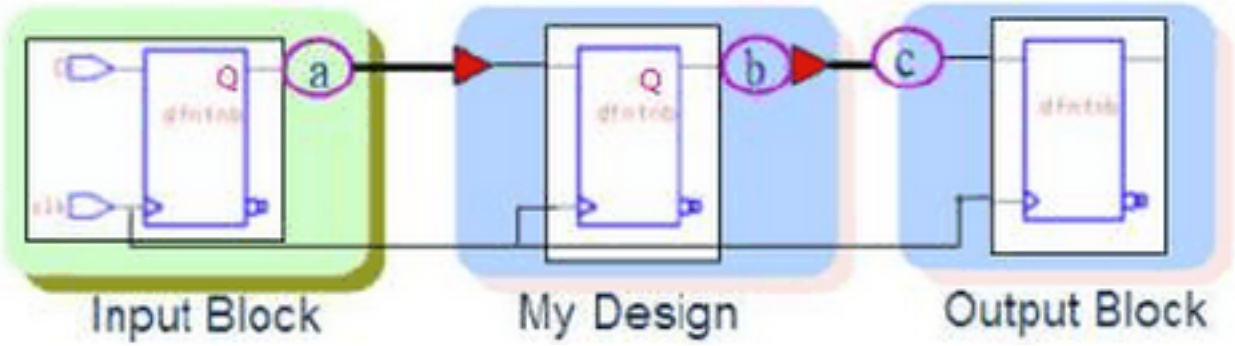
- Path
  - FF Clock to FF Input
  - PI (Primary Input) to FF Input
  - FF Clock to PO (Primary Output)
  - PI to PO



Static Timing Analysis

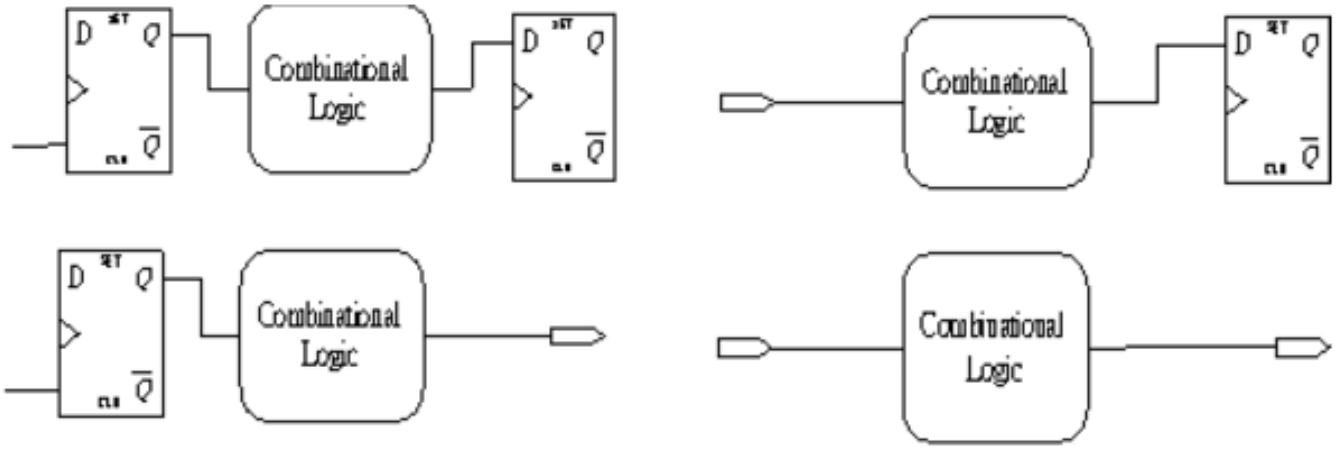
- Boundary Conditions: External Environment
  - driving cell
  - input transition time
  - output capacitance load
  - input delay
  - output delay



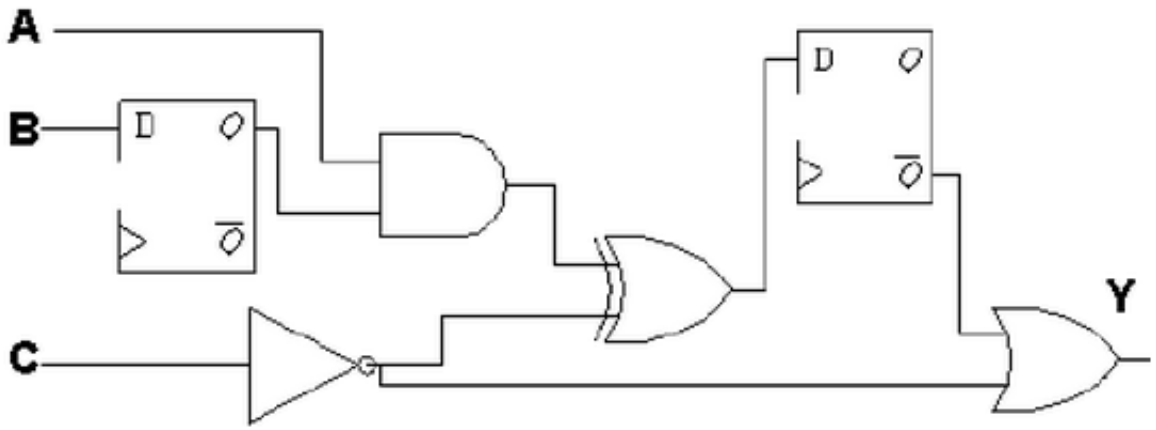


Static Timing Analysis

- Once boundary condition is defined, all four types of paths can be converted into the 1st type of path



STA Example

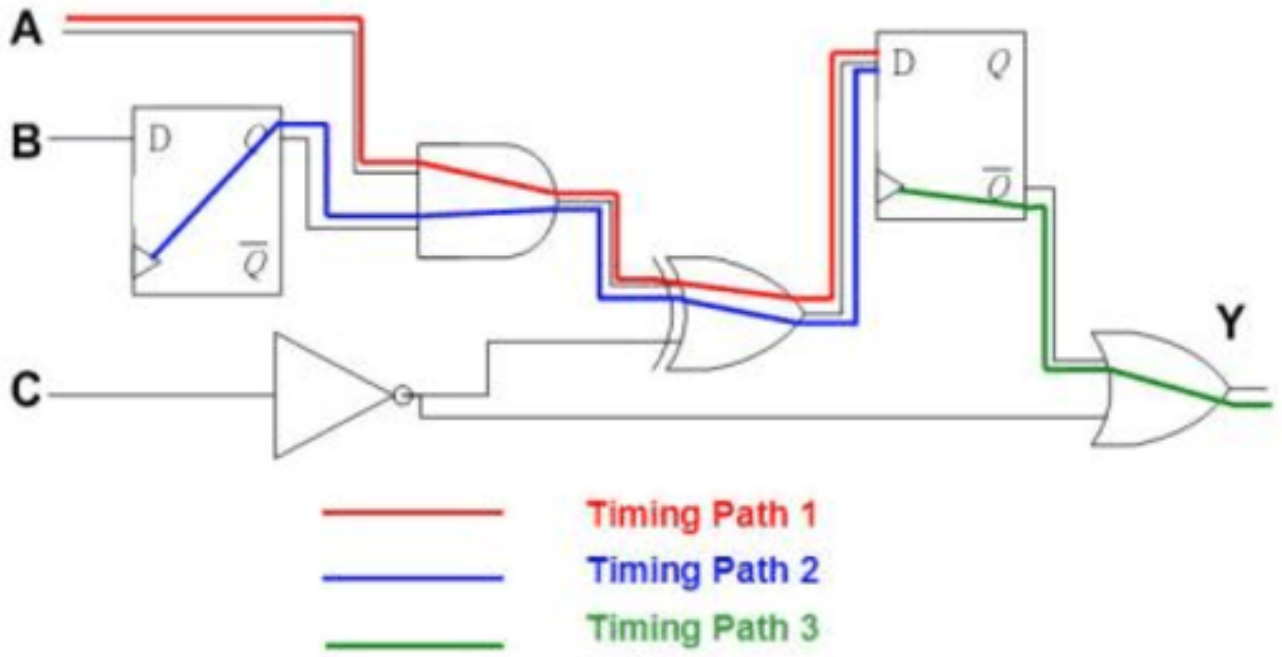


- Timing Model

Gate 0-1	3ns	FF Setup	1ns	Clock N.L. (Dclkn)	3ns
Gate 1-0	2ns	FF Hold	1ns	Clock Uncertainty (Dclku)	1ns
Net	2ns	Clock	14ns	Input Delay (Da, Db, Dc)	1ns
FF CLK-Q	3ns	Clock S.L. (Dclks)	2ns	Output Delay (DY)	3ns

STA Example

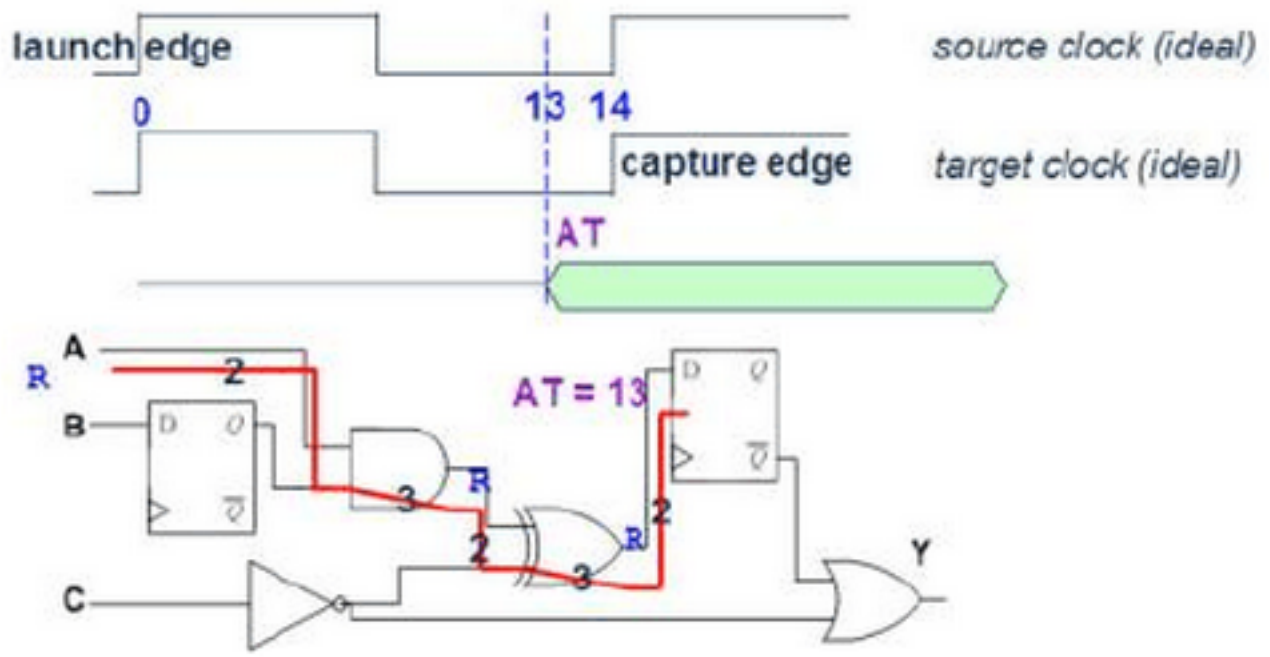
- Find Timing Path



STA Example

- Path 1: Arrival Time when A: 0->1

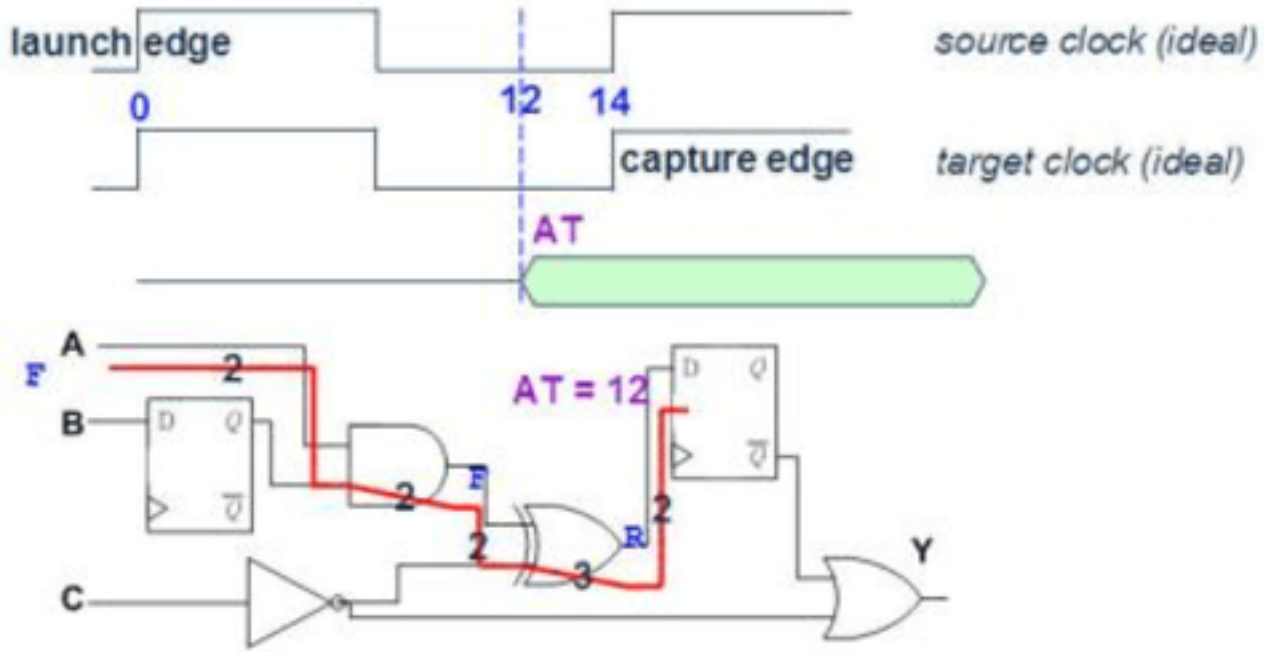
$$AT = D_a + 2 + 3 + 2 + 3 + 2 = 13ns$$



STA Example

- Path 1: Arrival Time when A : 1->0

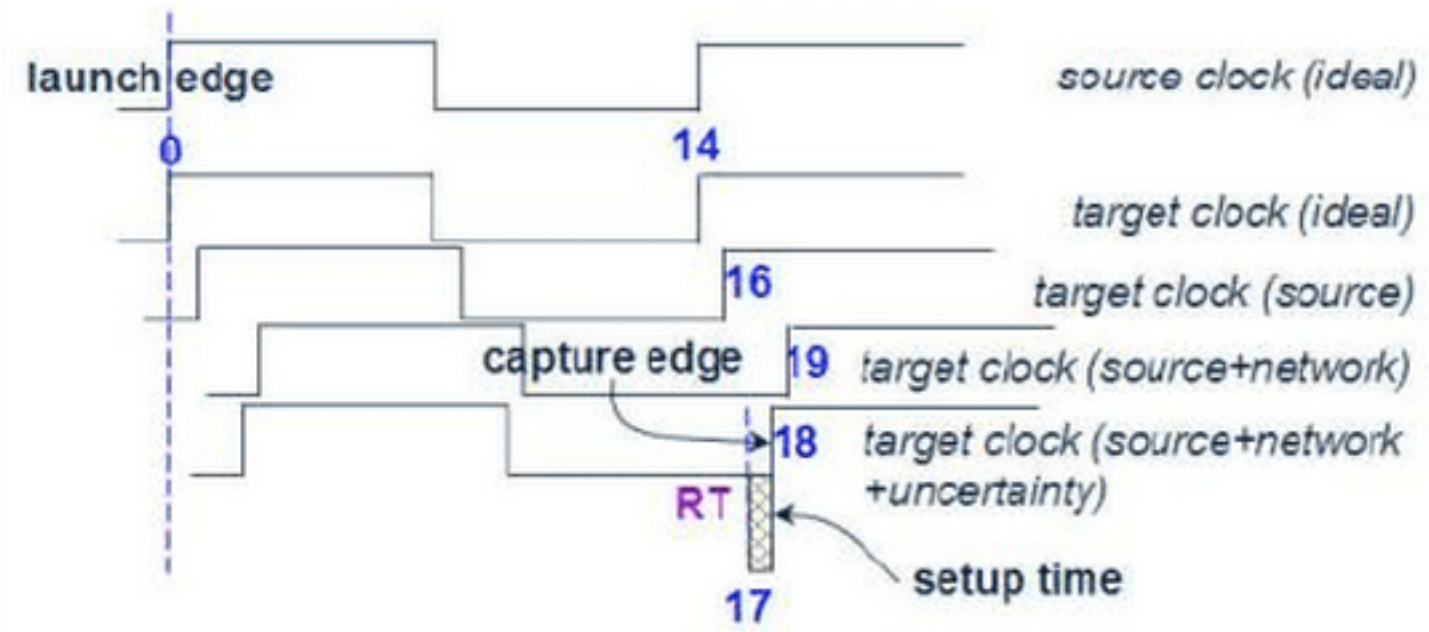
$$AT = D_a + 2 + 2 + 2 + 3 + 2 = 12ns$$



STA Example

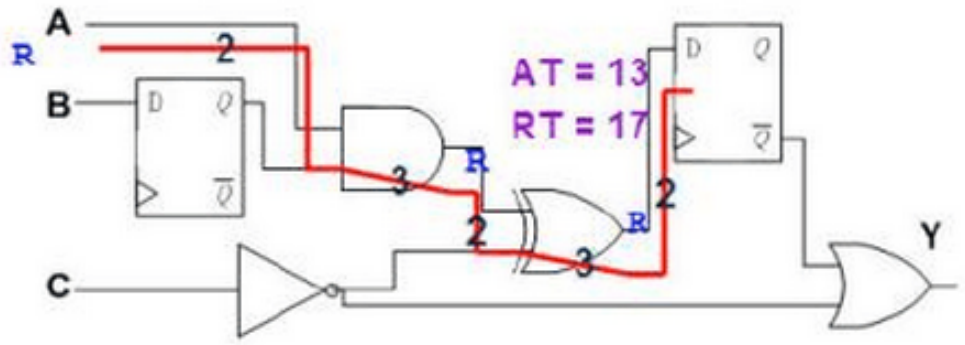
- Path 1: Required Time

$$RT = D_{clkp} + D_{clks} + D_{clkn} - D_{clku} - T_s = 14 + 2 + 3 - 1 - 1 = 17ns$$



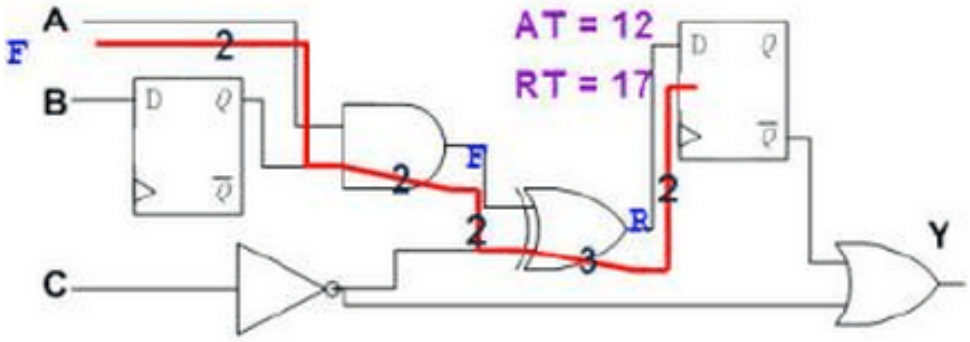
STA Example

- Path 1:
  - Slack 0->1
  - "+" = GOOD



$$Slack = RT - AT = 17 - 13 = 4ns$$

- Slack 1->0
- "+" = GOOD

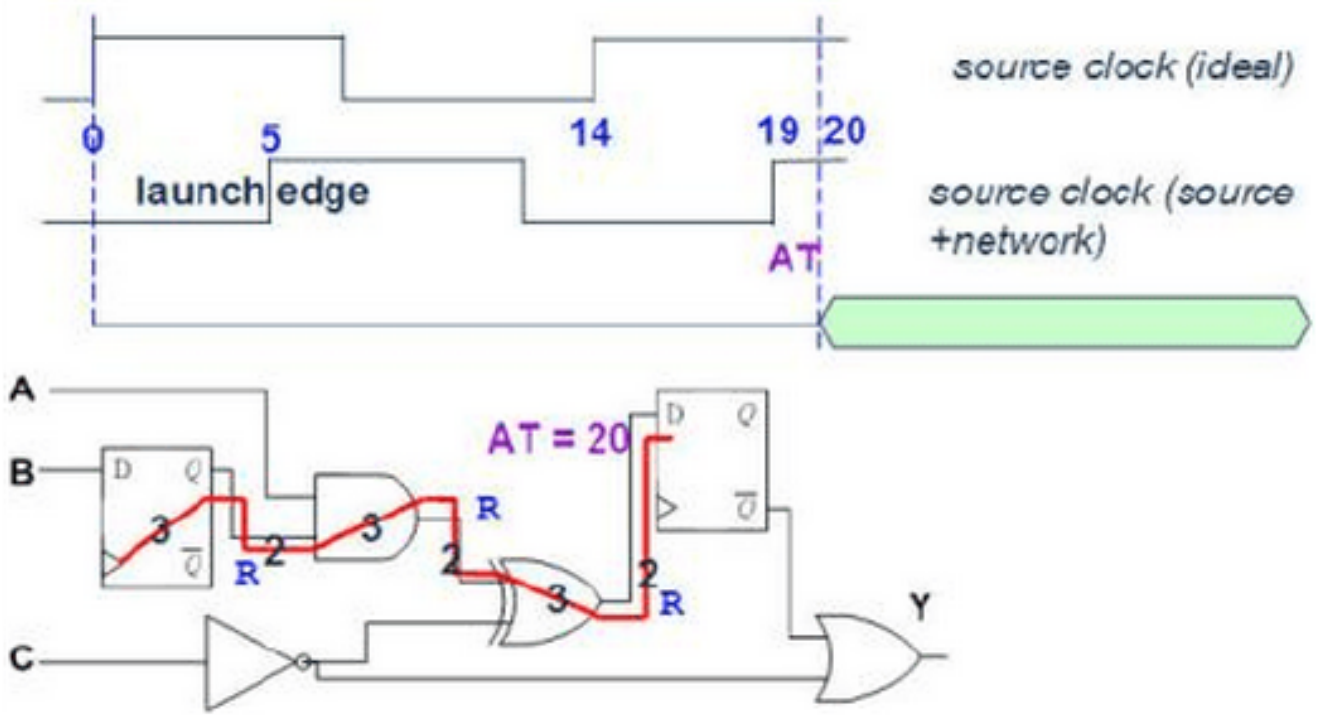


$$Slack = RT - AT = 17 - 12 = 5ns$$

STA Example

- Path 2: Arrival Time when B: 0->1

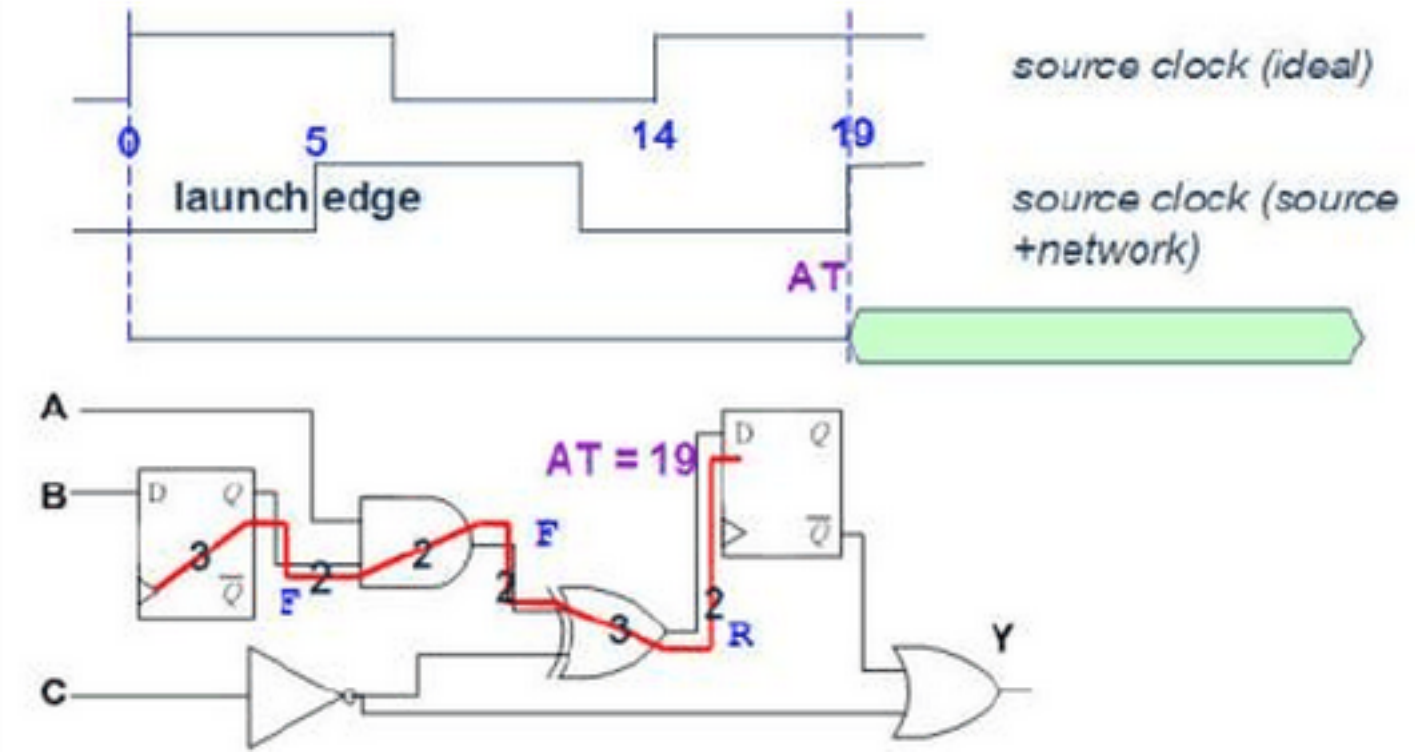
$$AT = D_{clks} + D_{clkn} + 3 + 2 + 3 + 2 + 3 + 2 = 20ns$$



STA Example

- Path 2: Arrival Time when B: 1->0

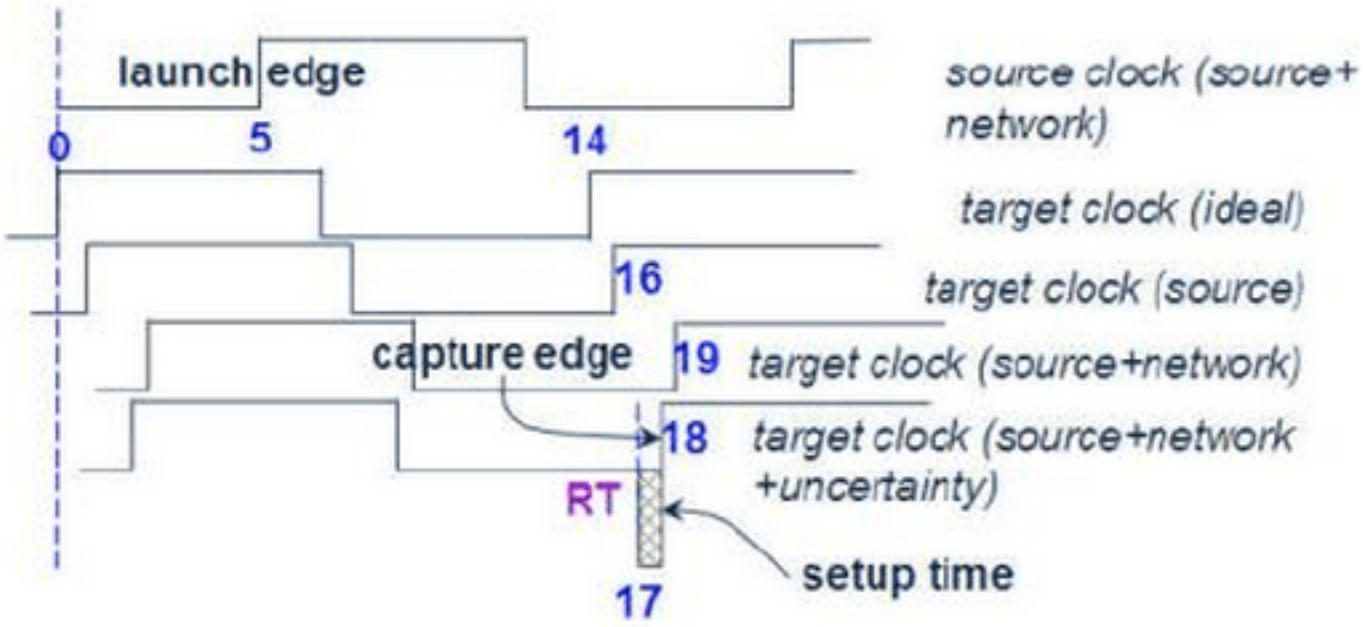
$$AT = D_{clks} + D_{clkn} + 3 + 2 + 2 + 2 + 3 + 2 = 20ns$$



STA Example

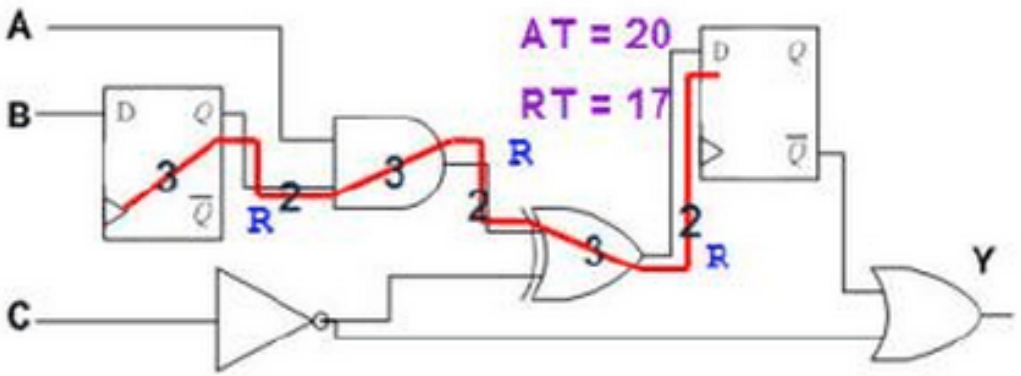
- Path 2: Required Time

$$RT = D_{clkp} + D_{clks} + D_{clkn} - D_{clku} - T_s = 14 + 2 + 3 - 1 - 1 = 17ns$$



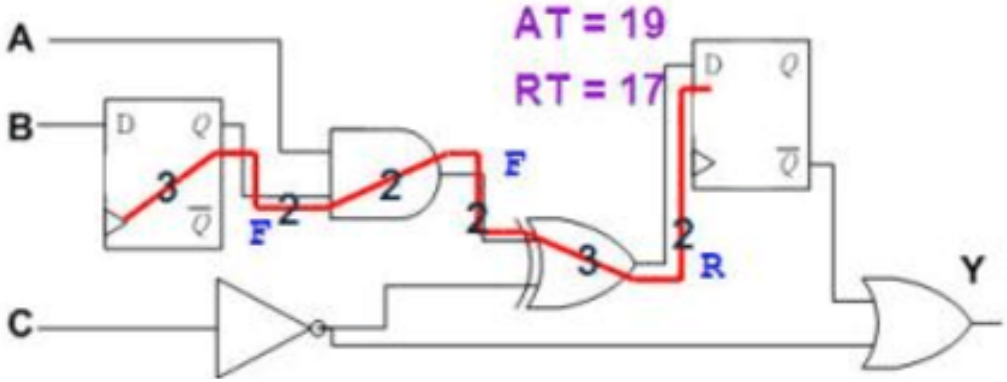
STA Example

- Path 2:
  - Slack 0->1
  - "—" = BAD



$$Slack = RT - AT = 17 - 20 = -3$$

  - Slack 1->0
  - "—" = BAD

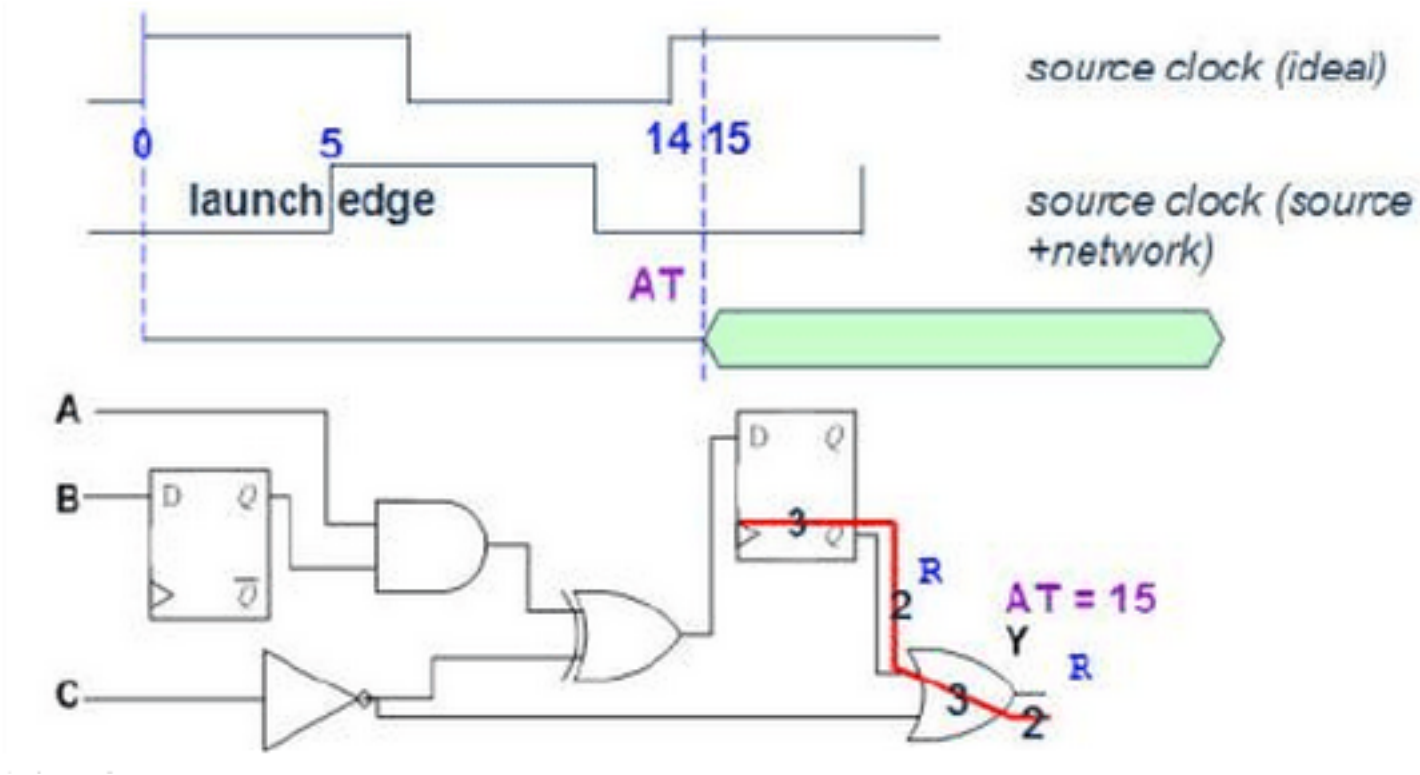


$$Slack = RT - AT = 17 - 19 = -2$$

STA Example

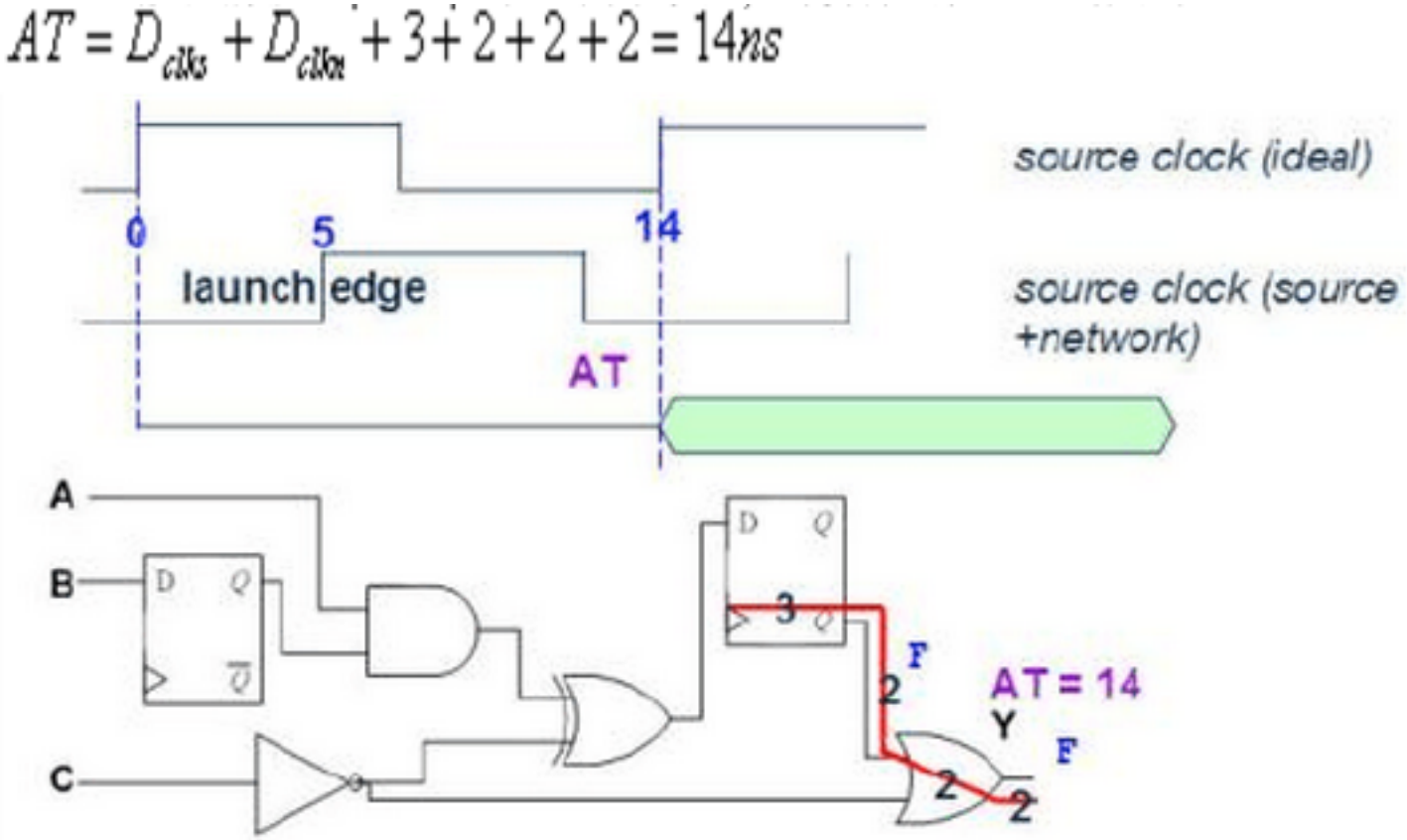
- Path 3: Arrival Time: 0->1

$$AT = D_{clks} + D_{clkn} + 3 + 2 + 3 + 2 = 15ns$$



STA Example

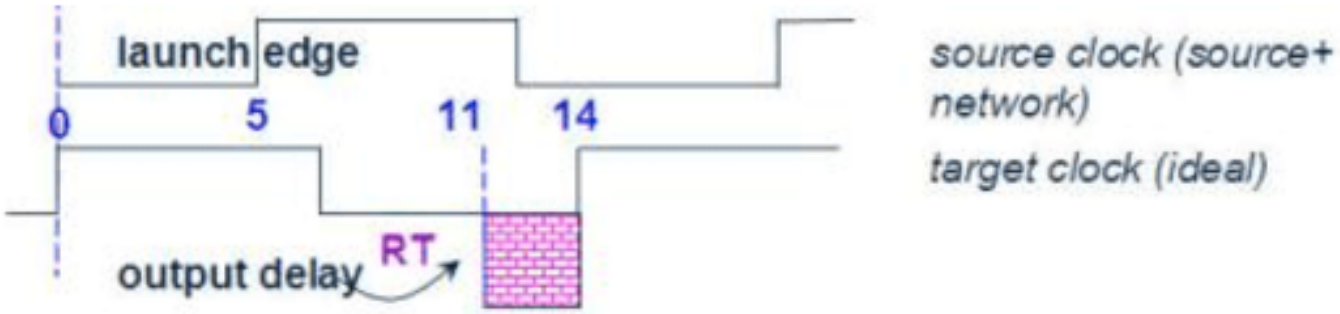
- Path 3: Arrival Time: 1->0

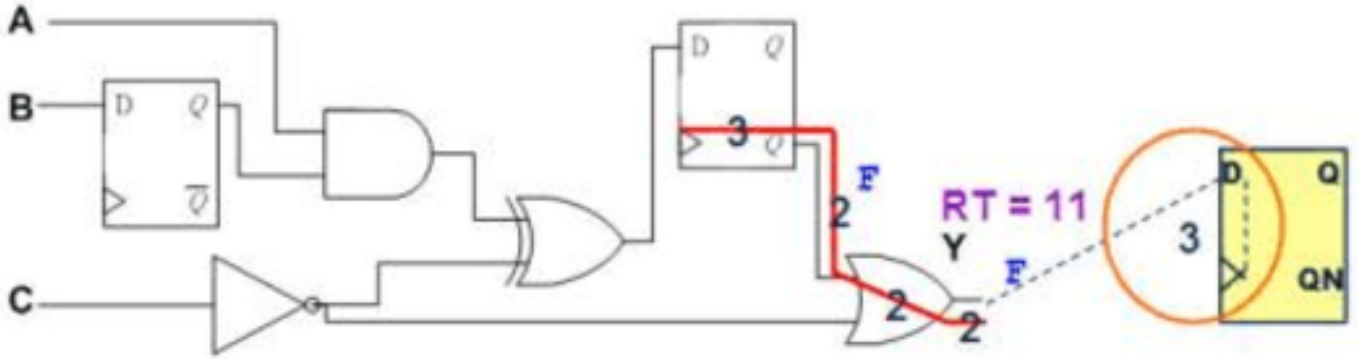


STA Example

- Path 3: Required Time

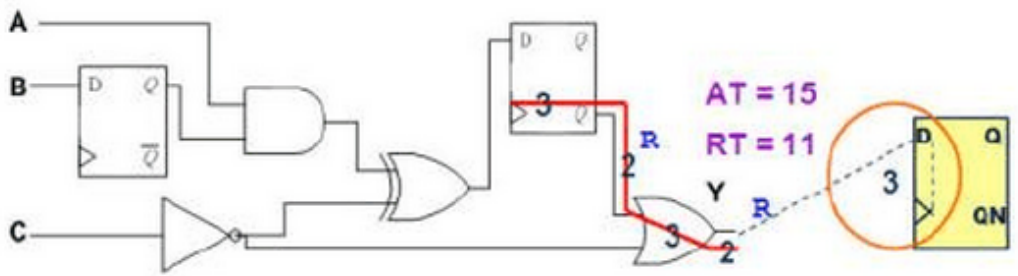
$$RT = D_{clkp} - D_Y = 14 - 3 = 11ns$$





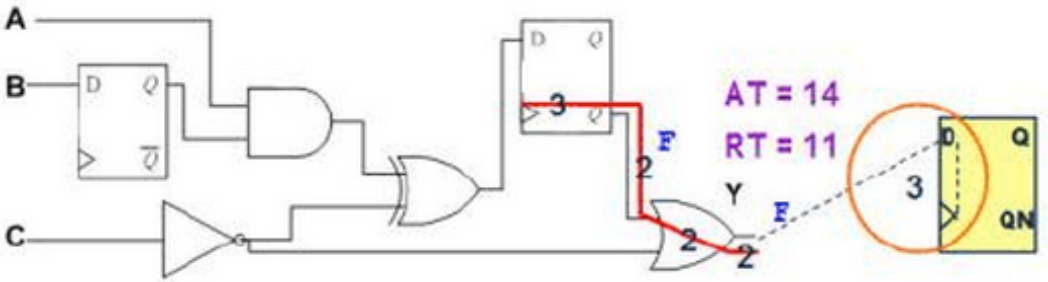
STA Example

- Path 3:
  - Slack 0->1
  - "—" = BAD



$$Slack = RT - AT = 11 - 15 = -4$$

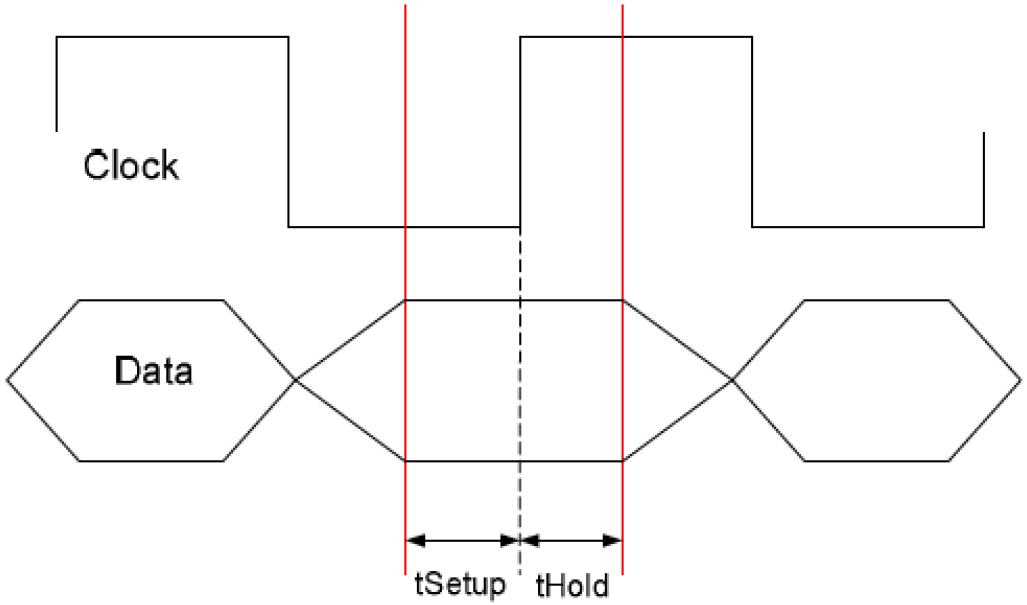
  - Slack 1->0
  - "—" = BAD



$$Slack = RT - AT = 11 - 14 = -3$$

Timing Violation

- Setup violations
- Hold violations
- Transition violations



Setup Time Violation

- Data path too slow compared to the clock speed at the latch edge

- Fix setup violations
  - reduce delay in data path
  - increase delay in clock
  - reduce number of buffers in the path
  - increase the size of buffers
  - reduce capacitance
  - reduce clock uncertainty
  - insert buffers for the clock
  - reduce clock speed (fix violation after tapeout)

Hold Time Violation

- Data not held long enough after latch edge
  - new data is too fast compared to the clock speed

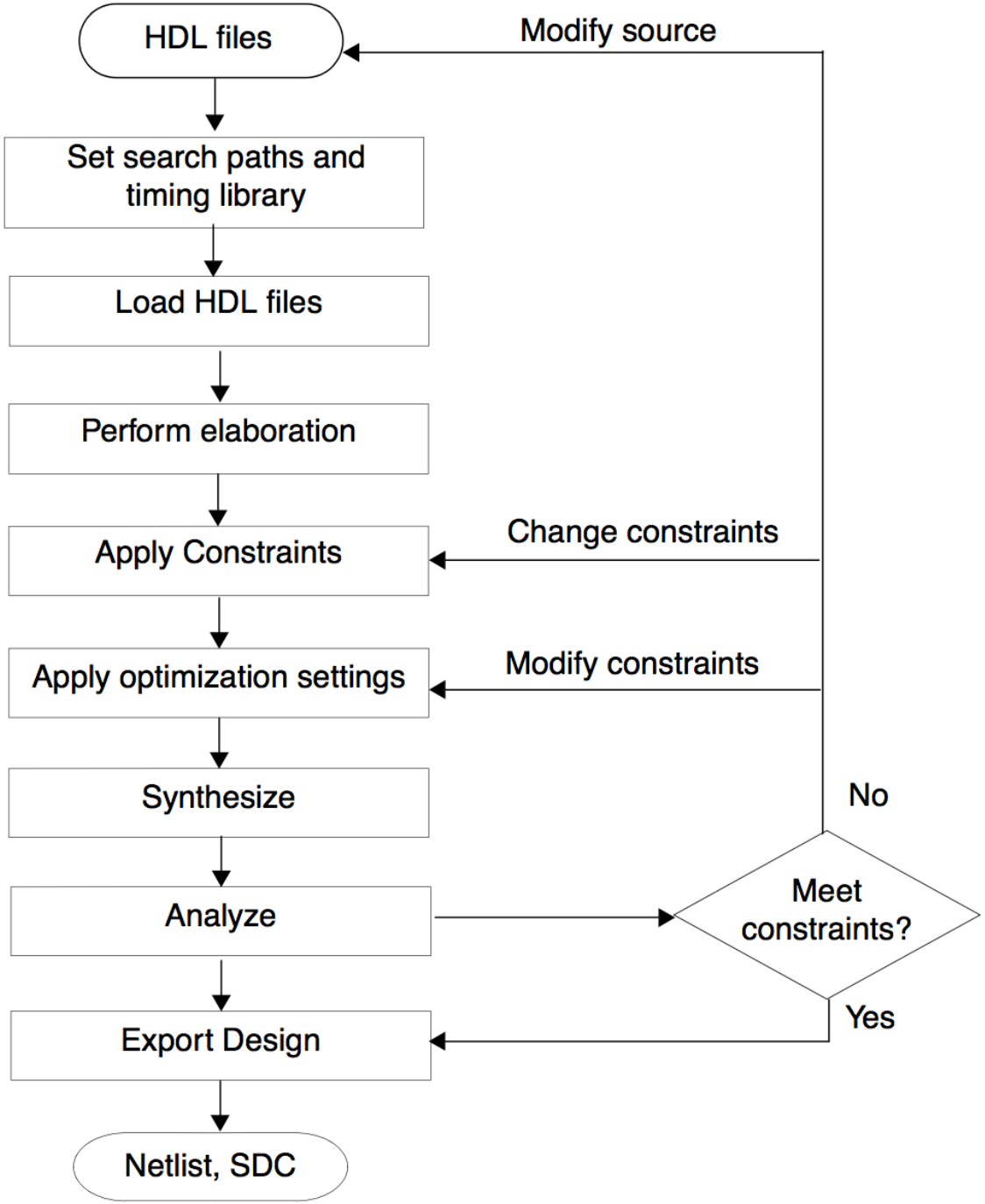
- Fix hold time violations
  - adding buffers to the data path
  - reduce buffer size in the data path
  - add more capacitance to the buffer output
  - time borrowing from setup time margin

After tapeout, no way to save hold time violation!

Transition Violations

- Signal takes too long transiting from one logic level to another
  - meta-stable

- Fix transition violations
  - modify data path, instead of adjusting register location, or adding buffers to the global clock; otherwise you cause more violations than you fix
  - reducing capacitance
  - adding a buffer
  - using more powerful device
  - reduce resistance (increase width of route)


HDL files
Modify source
Set search paths and timing library
Load HDL files
Perform elaboration
Apply Constraints
Change constraints
Apply optimization settings
Modify constraints
Synthesize
No
Analyze
Meet constraints?
Yes
Export Design
Netlist, SDC

Questions?

Comments?

Discussion?