Lecture 12
Timing Analysis, Part 1

Xuan ‘Silvia’ Zhang
Washington University in St. Louis

http://classes.engineering.wustl.edu/ese461/

Types of Simulation

higher level
less accurate
faster

- Behavioral simulation
  - black box with inputs and outputs
- Functional simulation
  - unit-delay simulation; ignore timing
- Static timing analysis
  - derive the longest delay path
- Gate-level simulation
  - aka. logic simulation; check ASIC timing performance
  - logic cell as black box modeled by functions with input signal as variables
- Switch-level simulation
- Transistor or circuit-level simulation

lower level
more accurate
slower

Static Timing Analysis

- "What is the longest delay in my circuit?"
  - critical path delay
  - determines the max clock frequency
- Dynamic analysis
  - vector-based simulation
  - find the input vector that activates the longest path
  - false path example
- Static timing
  - worst case analysis
  - no consideration of the input vector

Delay Models

- Timing vs delay model
  - timing model: delay outside the logic cells
  - delay model: delay inside the logic cells
- Types of delays
  - pin-to-pin: input pin to output pin, excluding interconnect
  - pin delay: delay lumped to pin
  - net/wire delay: interconnect
- Linear delay model
  - prop-ramp delay model

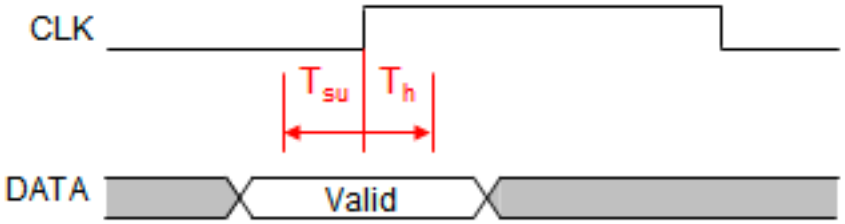
$$t_{PD} = R (C_{out} + C_p) + t_q$$

  - standard cell library data book

pin I (input) = 0.060 pF pin ZN (output) = 0.038 pF

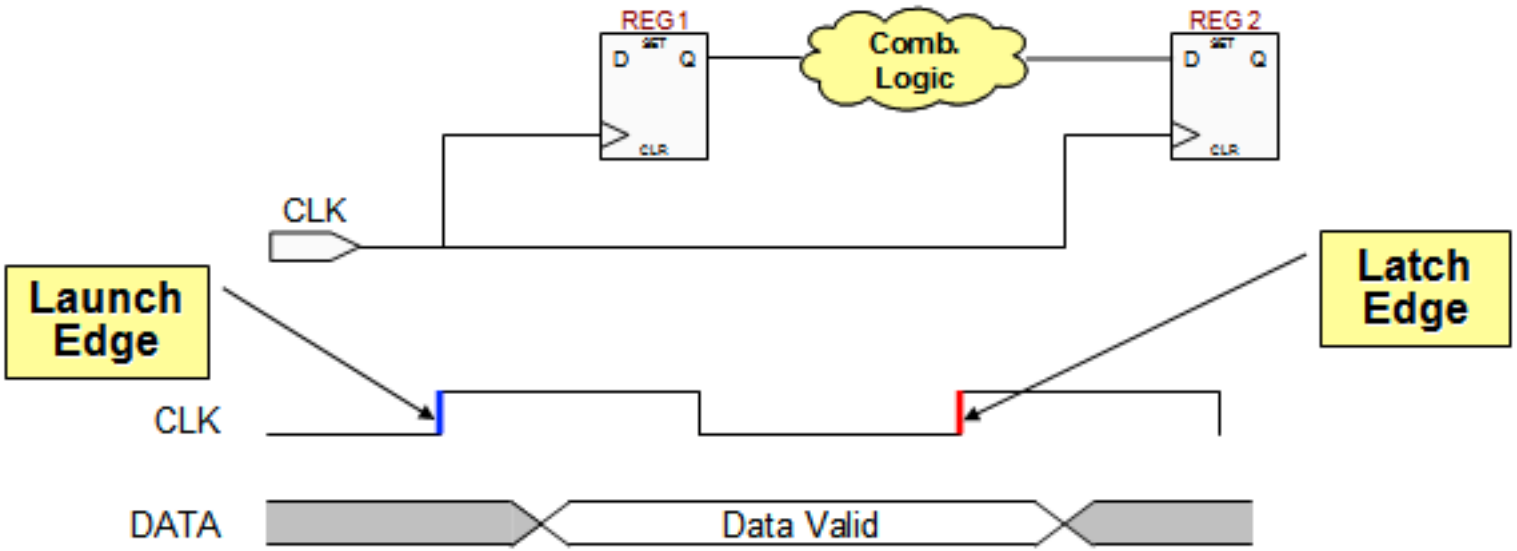
Timing in Digital Logic

- Setup time
- Hold time



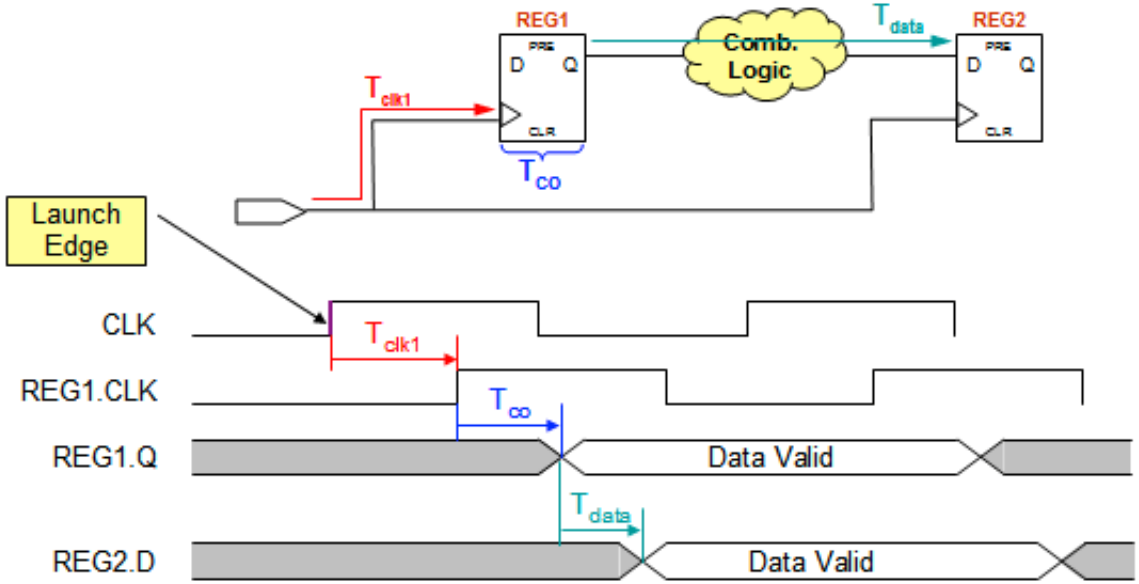
Timing in Digital Logic

- Launch edge and latch edge



Timing in Digital Logic

- Data arrival time: using launch edge

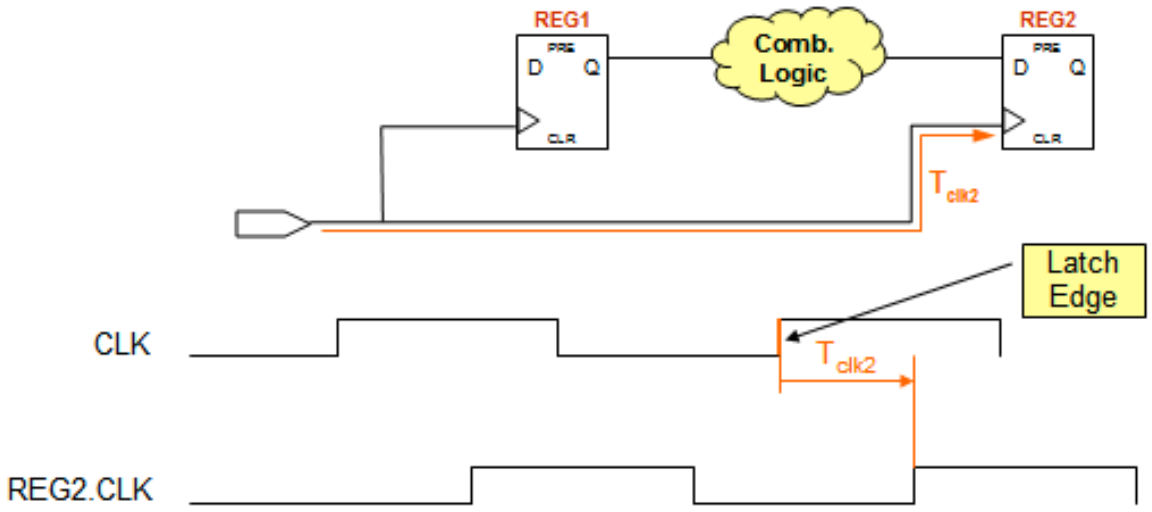


Data Arrival Time = launch edge + T_{clk1} + T_{co} +T_{data}

Tclk	Clock Skew	Tco	FF Clock-> Output	Tdata	Logic Delay

Timing in Digital Logic

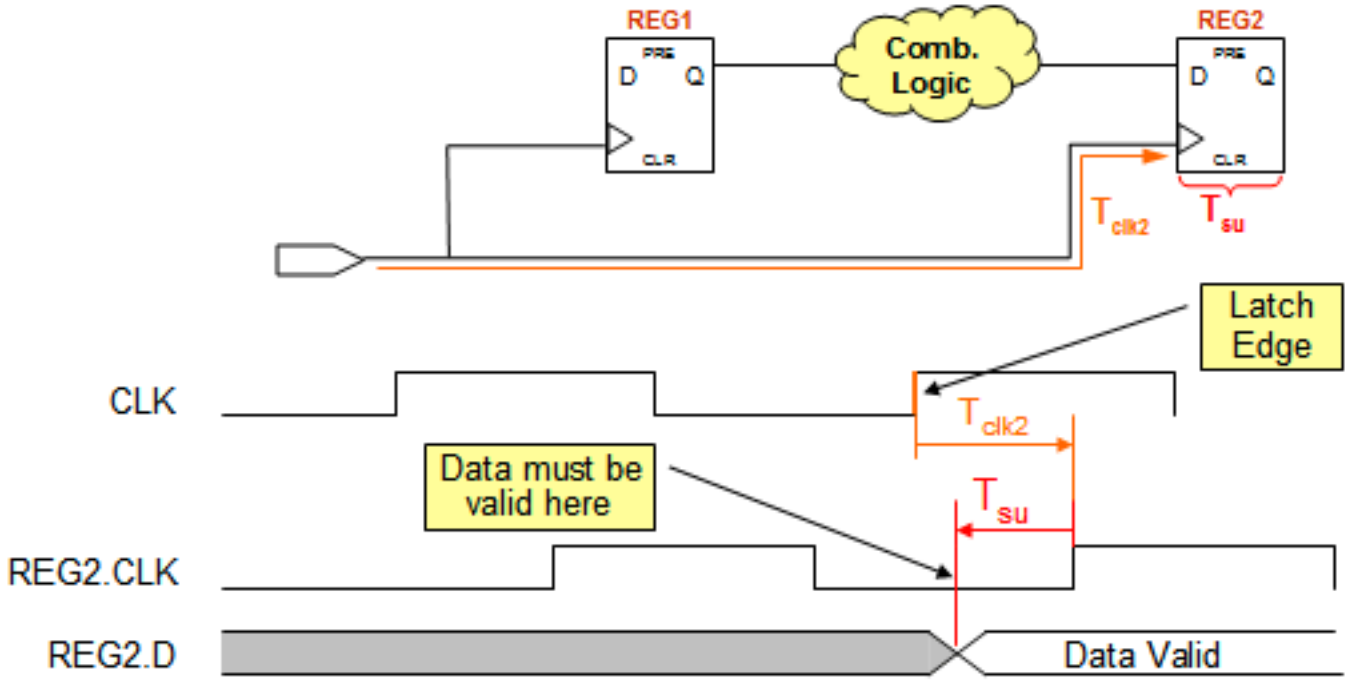
- Clock arrival time



Clock Arrival Time = latch edge + T_{clk2}

Timing in Digital Logic

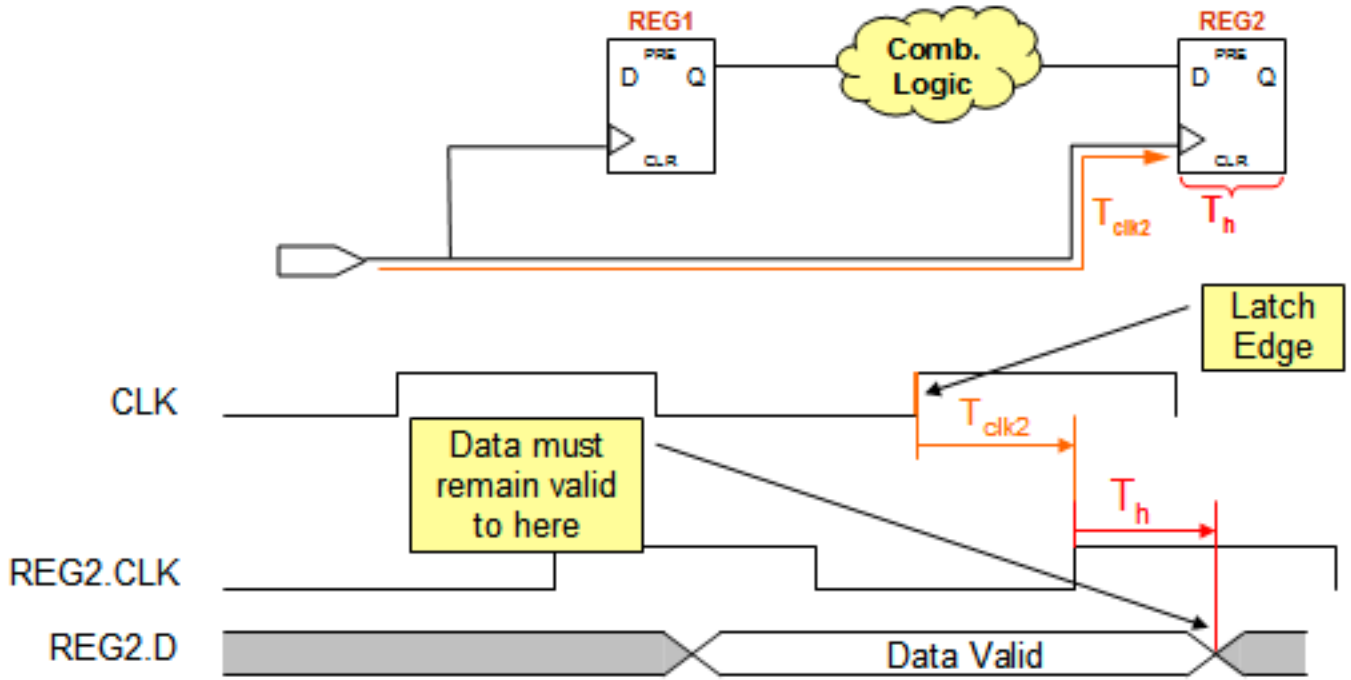
- Data required time (setup): latch edge



Data Required Time = Clock Arrival Time - T_{su} - Setup Uncertainty

Timing in Digital Logic

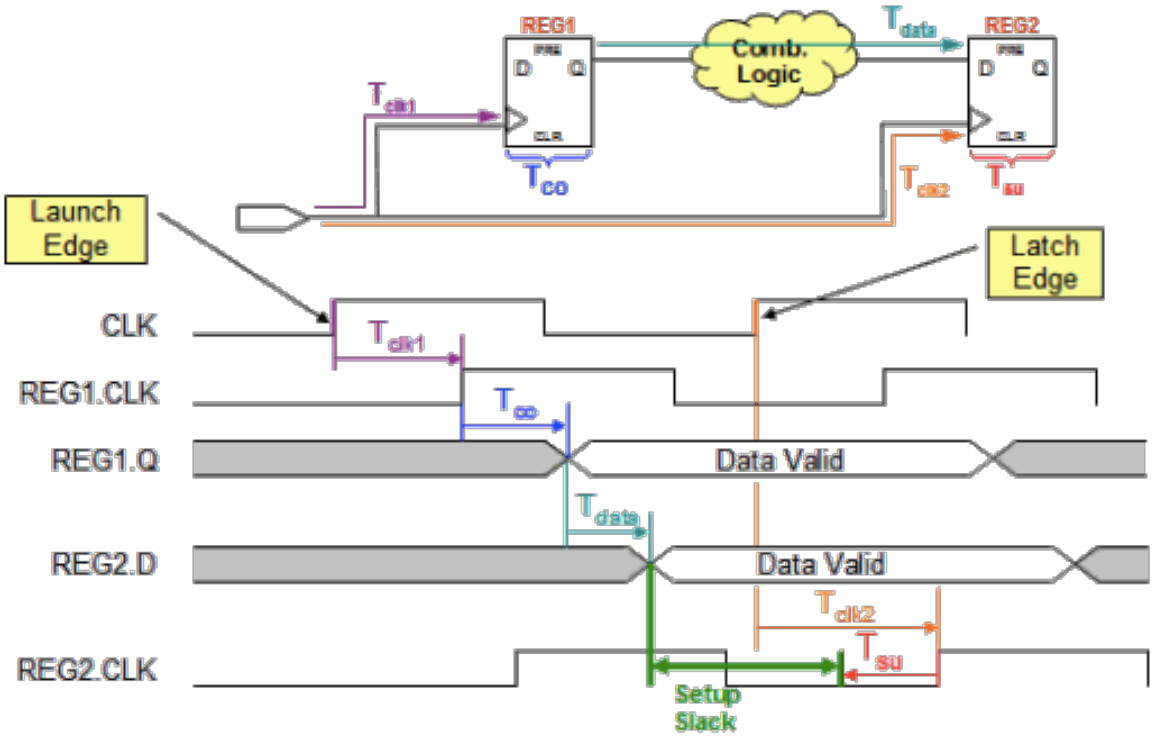
- Data required time (hold): next launch = latch



Data Required Time = Clock Arrival Time + T_h + Hold Uncertainty

Timing in Digital Logic

- Setup slack



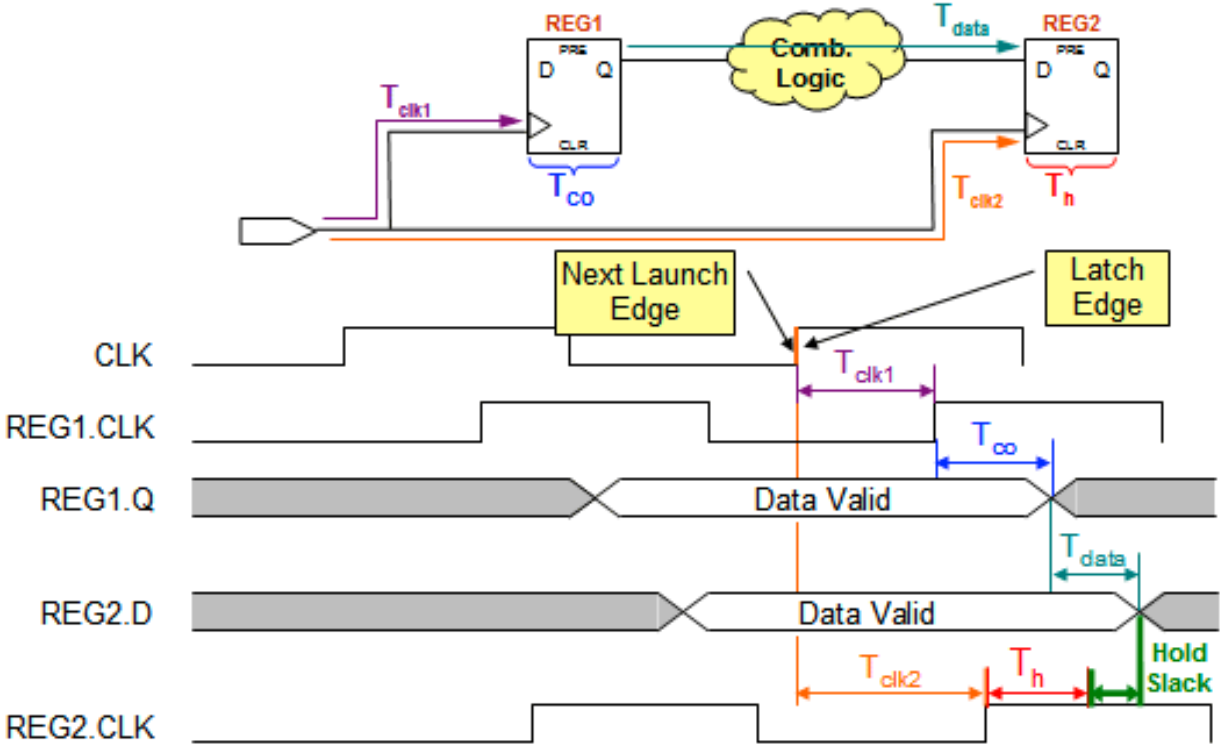
Setup Slack = Data Required Time – Data Arrival Time

Positive slack
Timing requirement me

Negative slack
Timing requirement not met

Timing in Digital Logic

- Hold slack



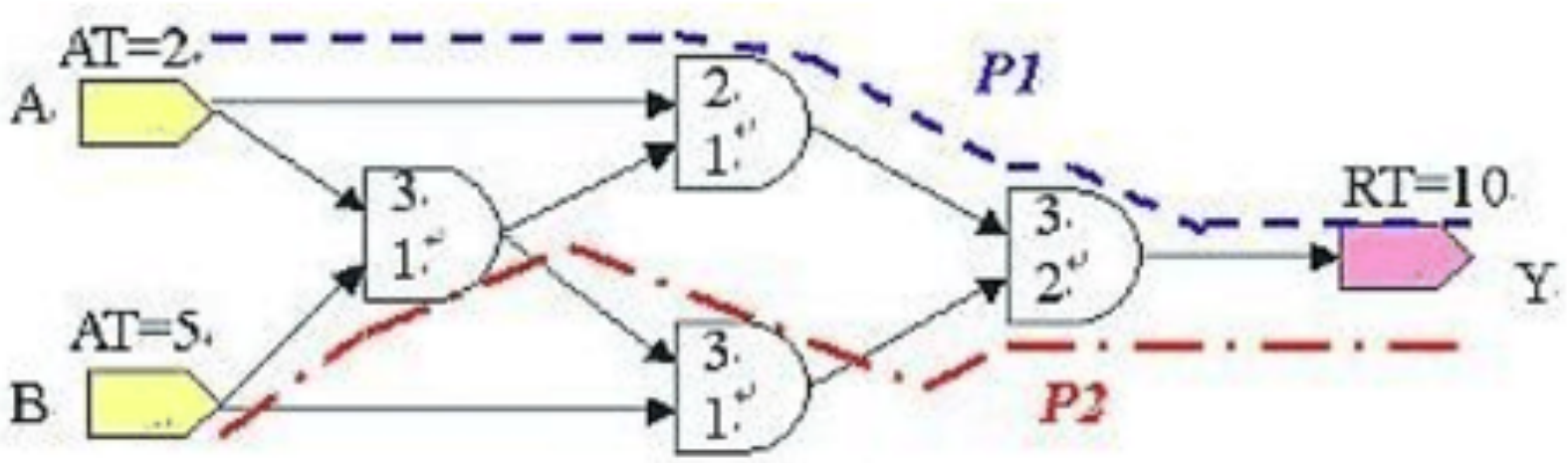
Hold Slack = Data Arrival Time – Data Required Time

Positive slack
Timing requirement me

Negative slack
Timing requirement not met

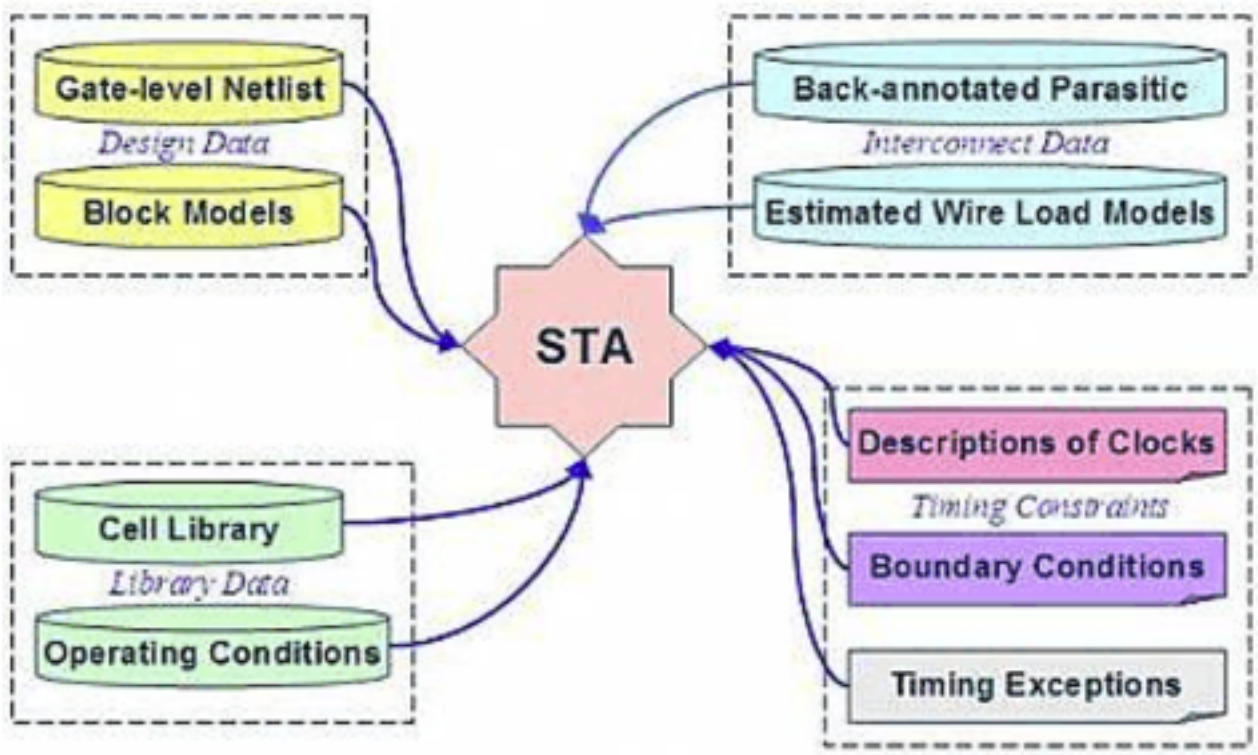
Static Timing Analysis

- Timing Model and Timing Constraint
- Arrival Time (AT) and Required Time (RT)



Static Timing Analysis

- Library Data

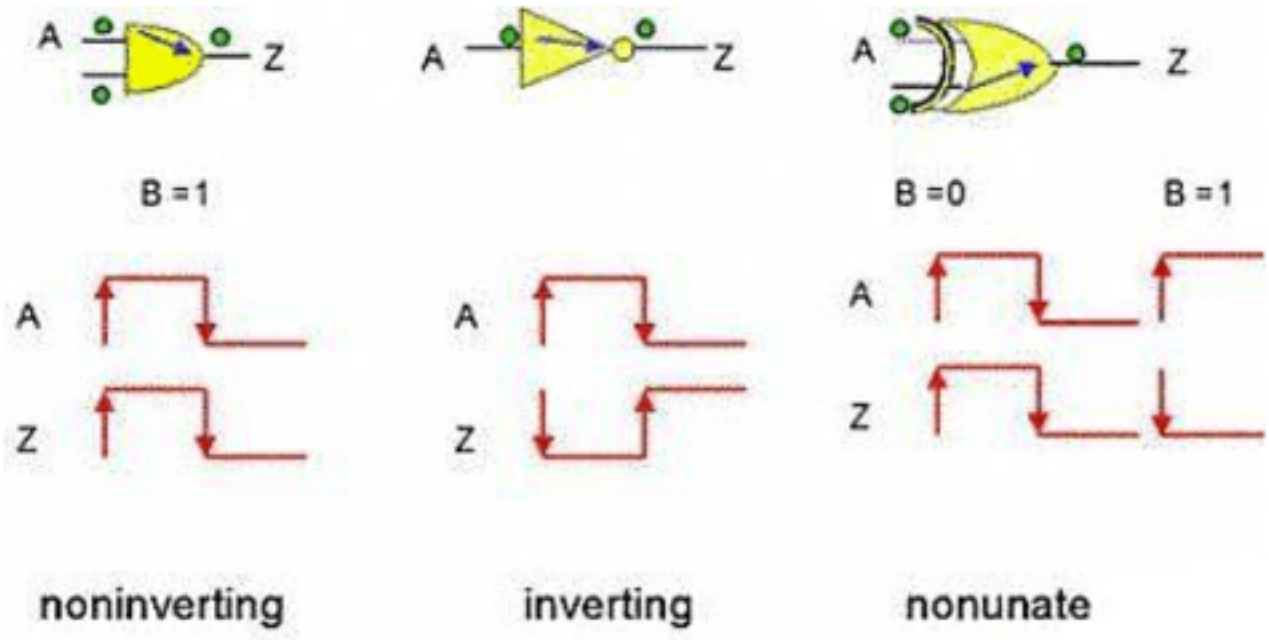


Static Timing Analysis

- Timing type
  - Combinational Timing (Delay)
  - Setup Timing (Check)
  - Hold Timing (Check)
  - Edge Timing (Delay)
  - Present and Clear Timing (Delay)
  - Recovery Timing (Check)
  - Removal Timing (Check)
  - Three State Enable & Disable Timing (Delay)
  - Width Timing (Check)

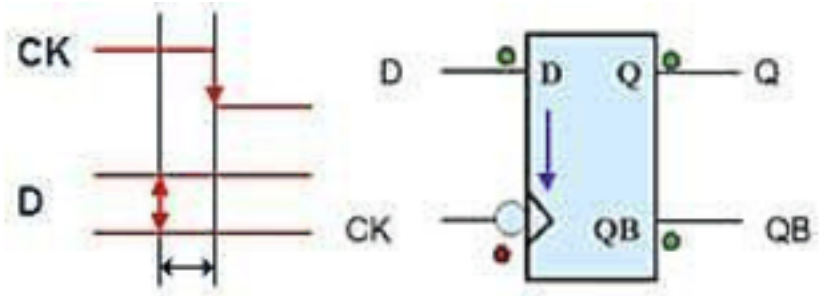
Static Timing Analysis

- Combinational Timing (Delay)

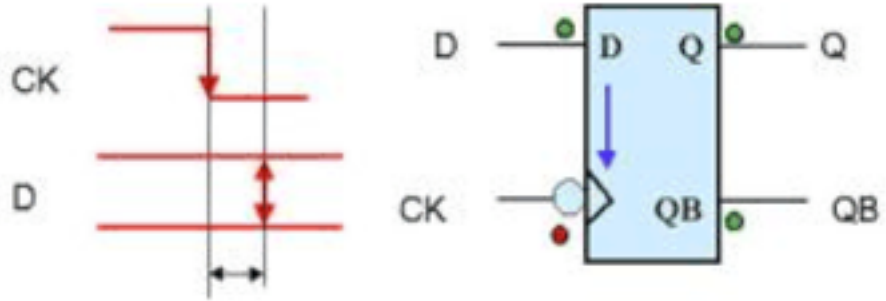


Static Timing Analysis

- Setup Timing (Check)

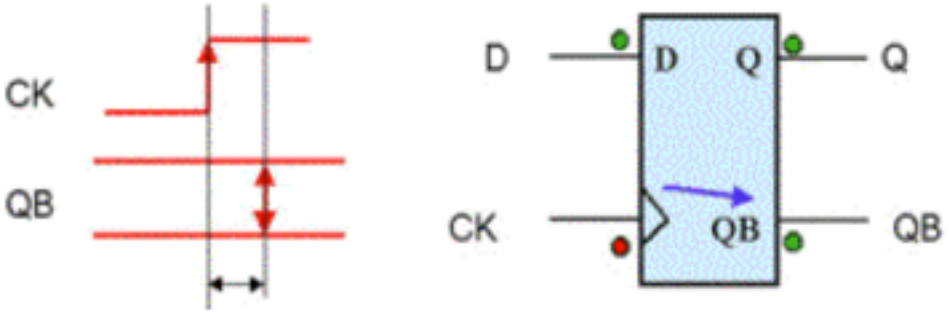


- Hold Timing (Check)

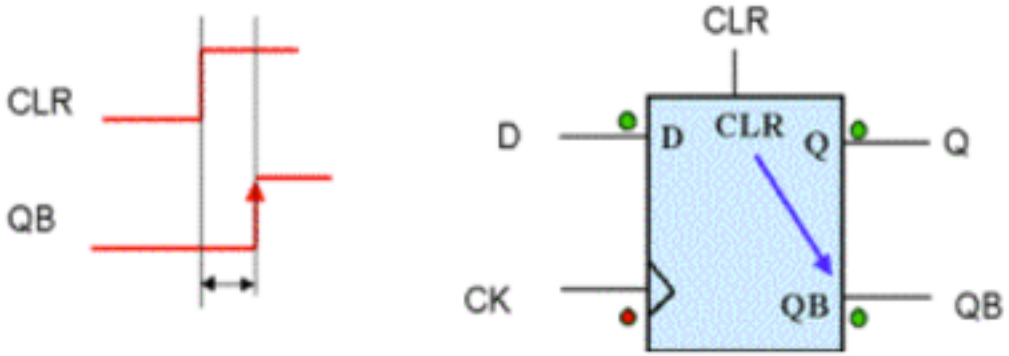


Static Timing Analysis

- Edge Timing (Delay)

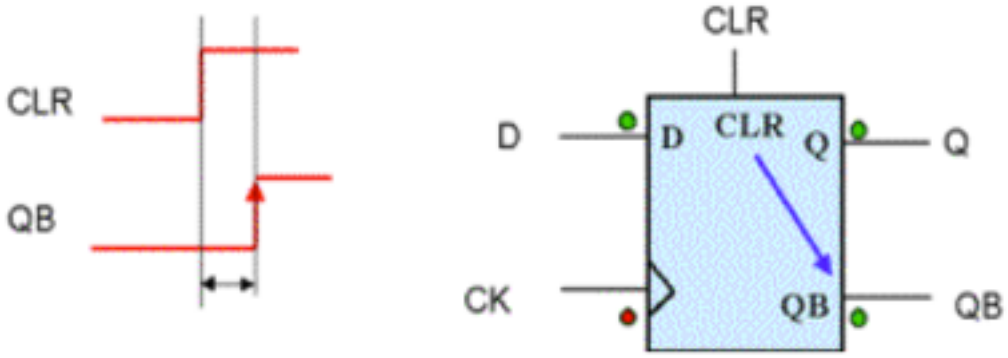


- Preset and Clear Timing (Delay)

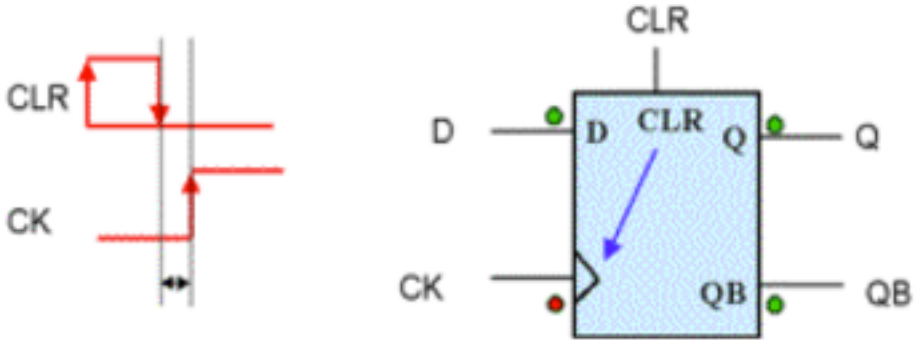


Static Timing Analysis

- Recovery Timing (Check)

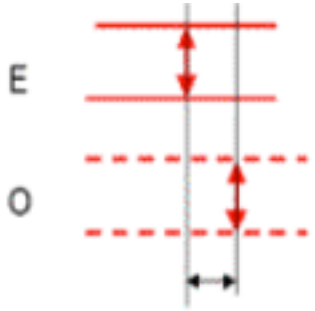


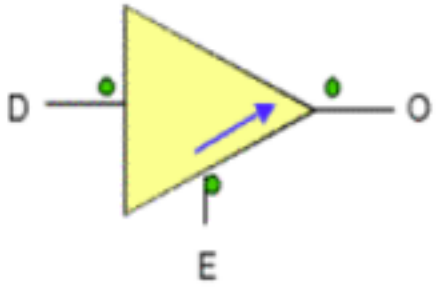
- Removal Timing (Check)



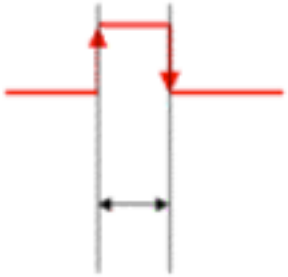
Static Timing Analysis

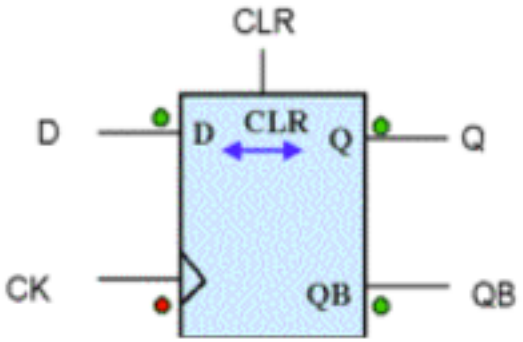
- Three State Enable & Disable Timing (Delay)





- Width Timing (Check)





Static Timing Analysis

- Interconnect Delay
  - Depends on P&R (Place and Routing)
  - Wireload Model: Fan-out
  - RC Extraction
  - Back-annotate for STA

Reference

- Chapter 13 from the ASIC book

Questions?

Comments?

Discussion?