Lecture 4
Review on Digital Logic (Part 3)

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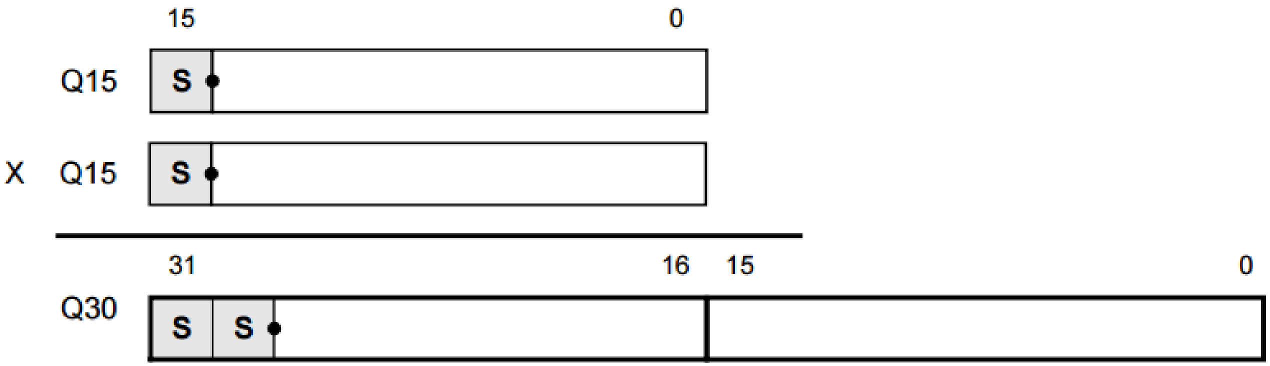
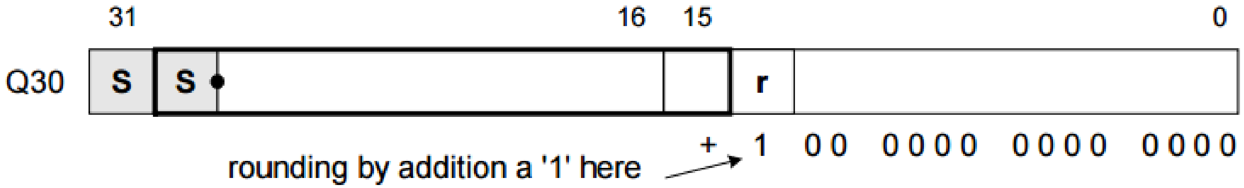
http://classes.engineering.wustl.edu/ese461/

Fixed Point Multiplication

- Two Q15 number multiply
  - Q15 × Q15 = Q30
  - 2.30 format, 32 bits, two sign bits
  - MSB: extended sign bit

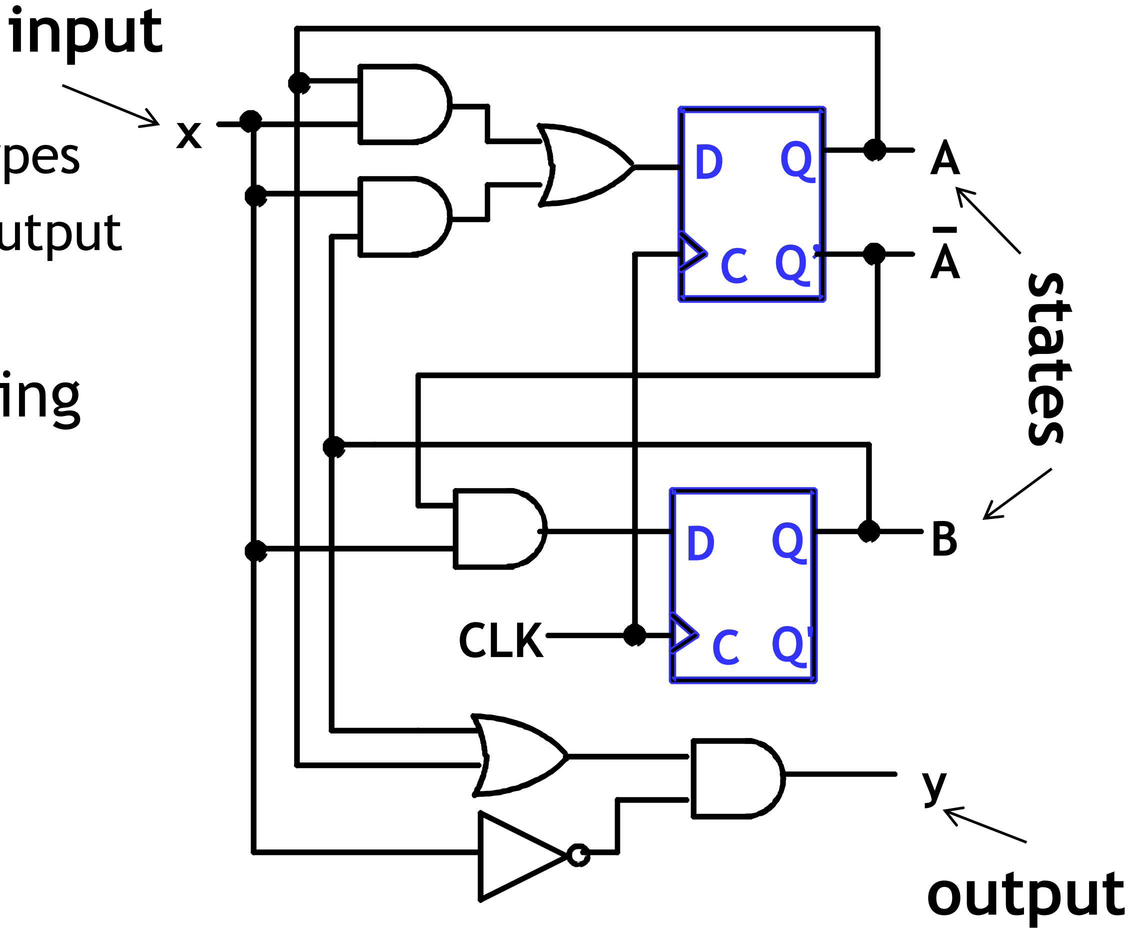


  - need to truncate back to 1.15 format
  - left shift by one bit, storing upper 16 bits
  - right shift by 15 bits, storing lower 16 bits



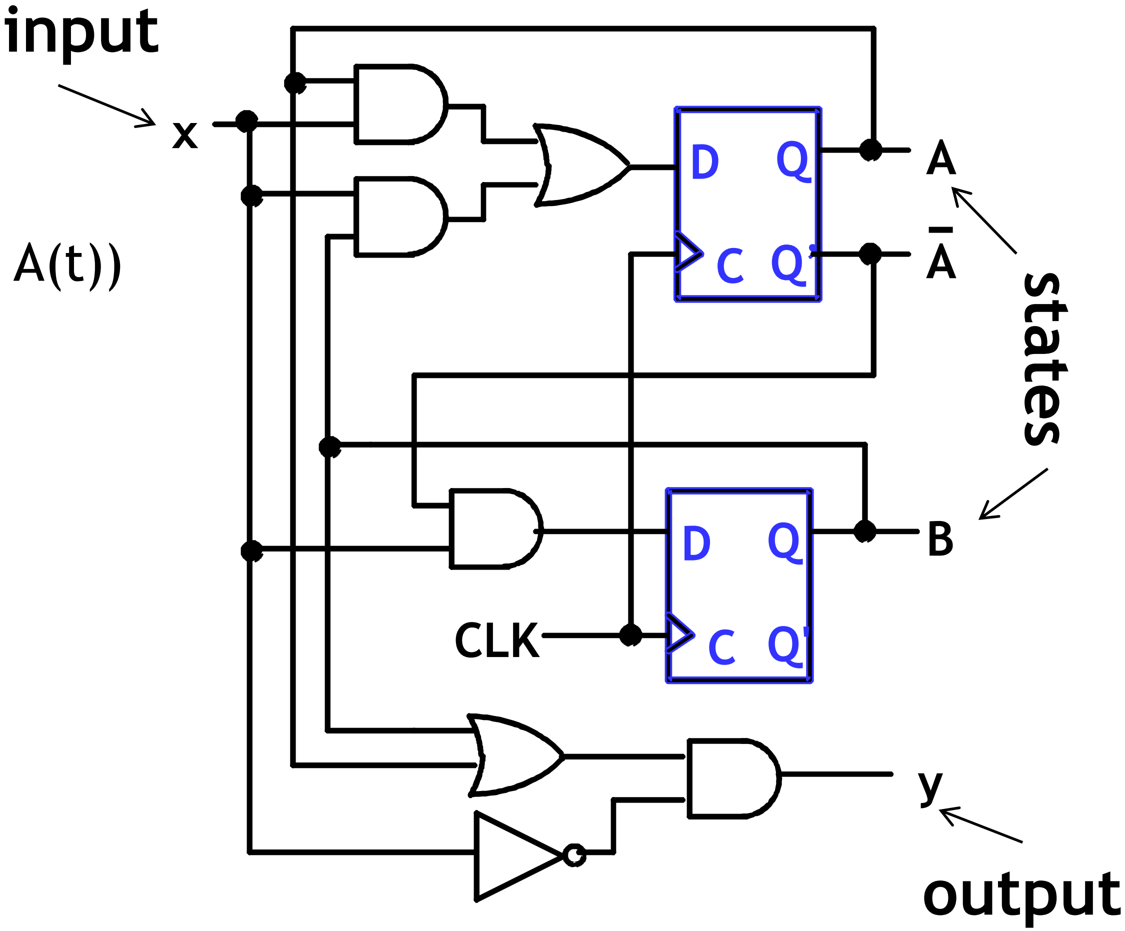
Sequential Circuit Analysis

- Design steps
  - word description
  - state diagram
  - state table
  - select flip-flop types
  - input to FF and output
  - verification
- Reverse engineering



Input Equations

- To flip-flops
  - $D_A = A(t)x(t)+B(t)x(t)$
  - $D_B = /A(t)x(t)$
- Output y
  - $y(t) = /x(t)(B(t) + A(t))$



State Table

- For the example: $A(t+1) = A(t)x(t) + B(t)x(t)$

  $B(t+1) = /A\ (t)x(t)$

  $y(t) = /x\ (t)(B(t) + A(t))$

Inputs of the table

Outputs of the table

2^3 rows

(2^{m+n}) rows

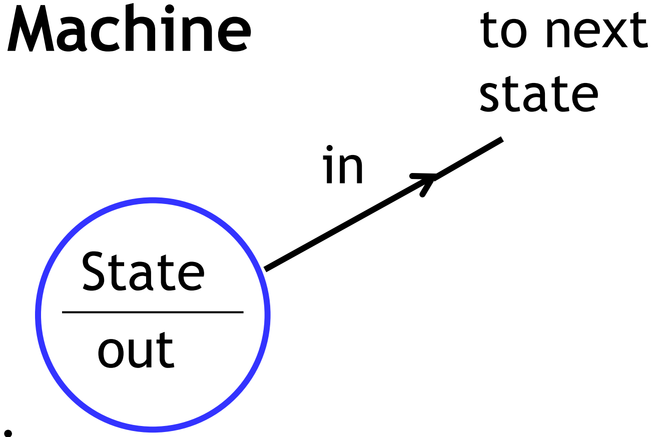
m: no. of FF
n: no. of inputs

Present State		Input	Next State		Output
A(t)	B(t)	x(t)	A(t+1)	B(t+1)	y(t)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

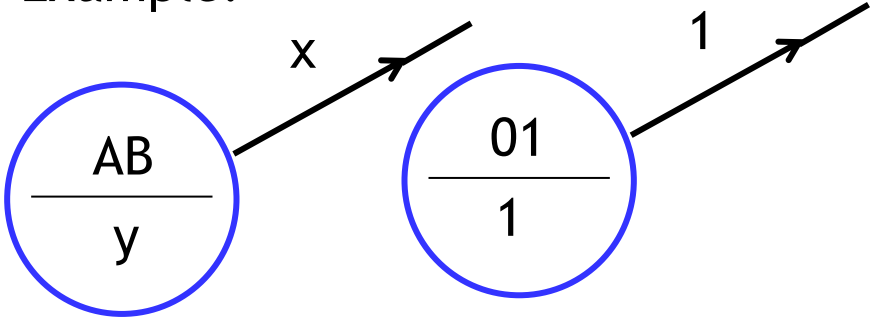
State Diagram

- Conventions

Moore Machine

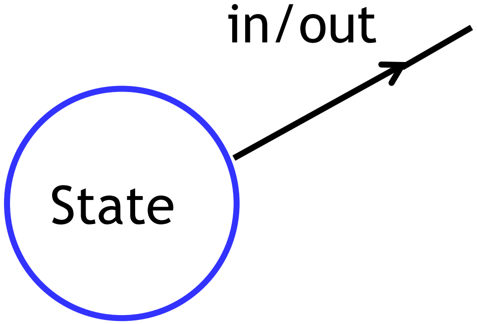


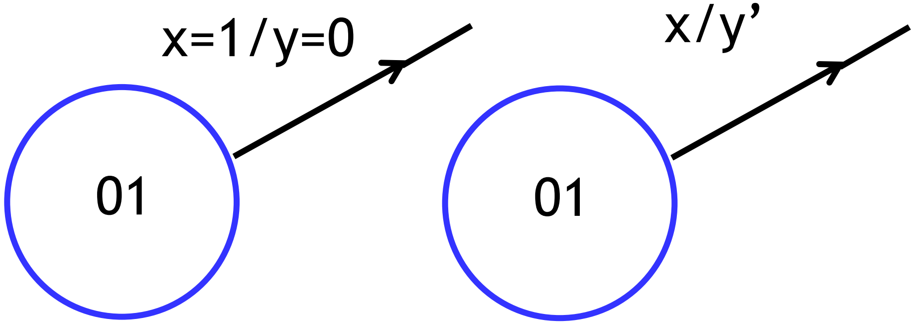
Example:



Moore type output depends only on state

Mealy Machine





Mealy type output depends on state and input

Example: Elevator Controller

- Description of the controller
  - elevator can be at one of two floors: ground and first
  - one button controls the elevator: up and down
  - two lights floor indicator: red (ground), green (1st)
- State diagram
- State table
- Boolean expressions

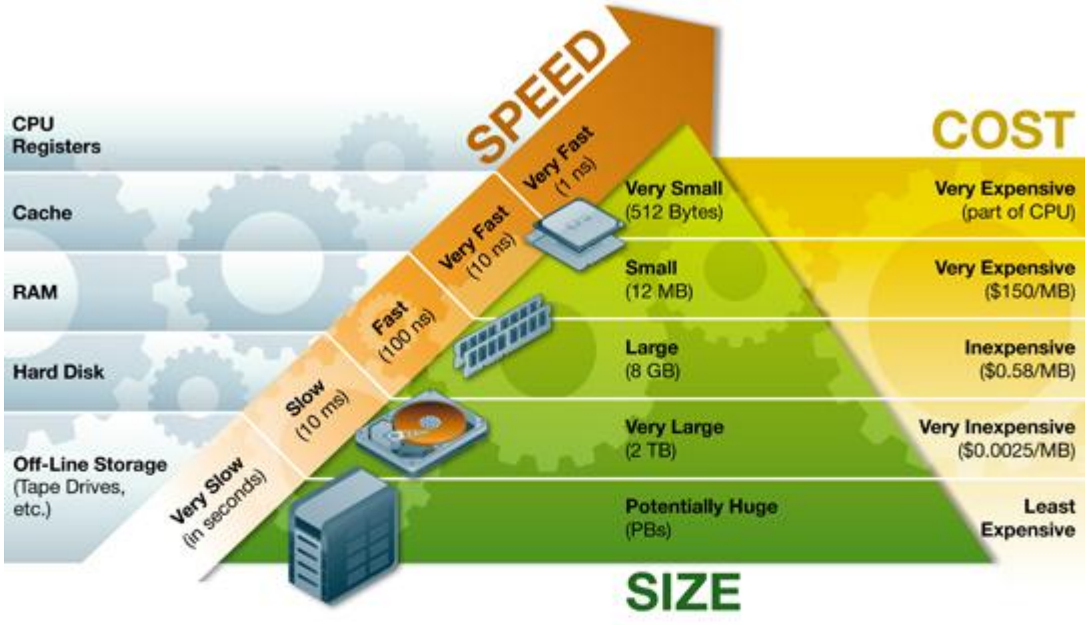
Outline

Arithmetic Logic

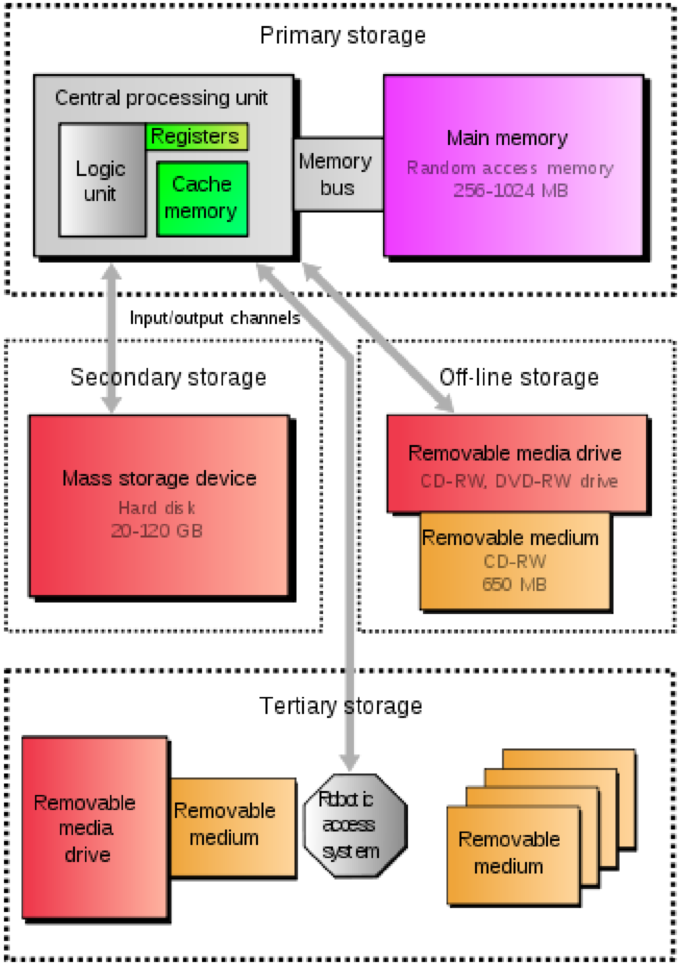
Sequential Logic

Memory Circuit

Memory Devices and Hierarchy



source: copterj.tumblr.com



source: wikipedia

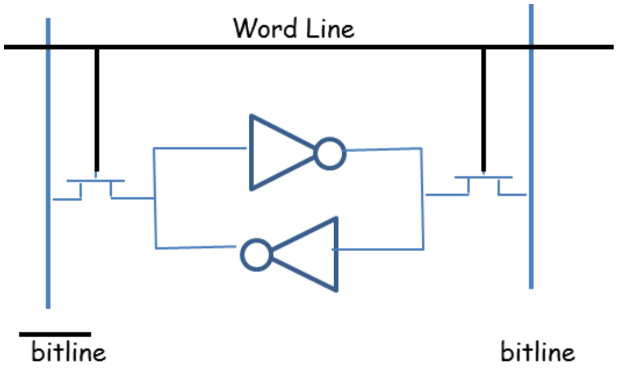
Static RAM

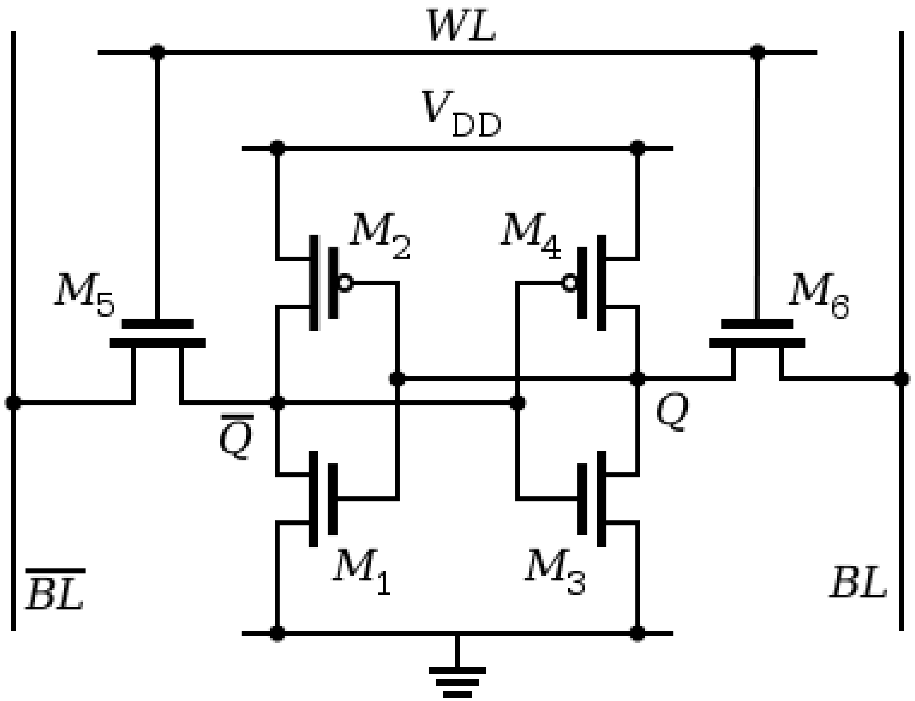
- Applications
  - CPU register file, cache, embedded memory, DSP

- Characteristics
  - 6 transistor per cell, other topologies
  - no need to refresh
  - access time ~ cycle time
  - no charge to leak
  - faster, more area, more expensive

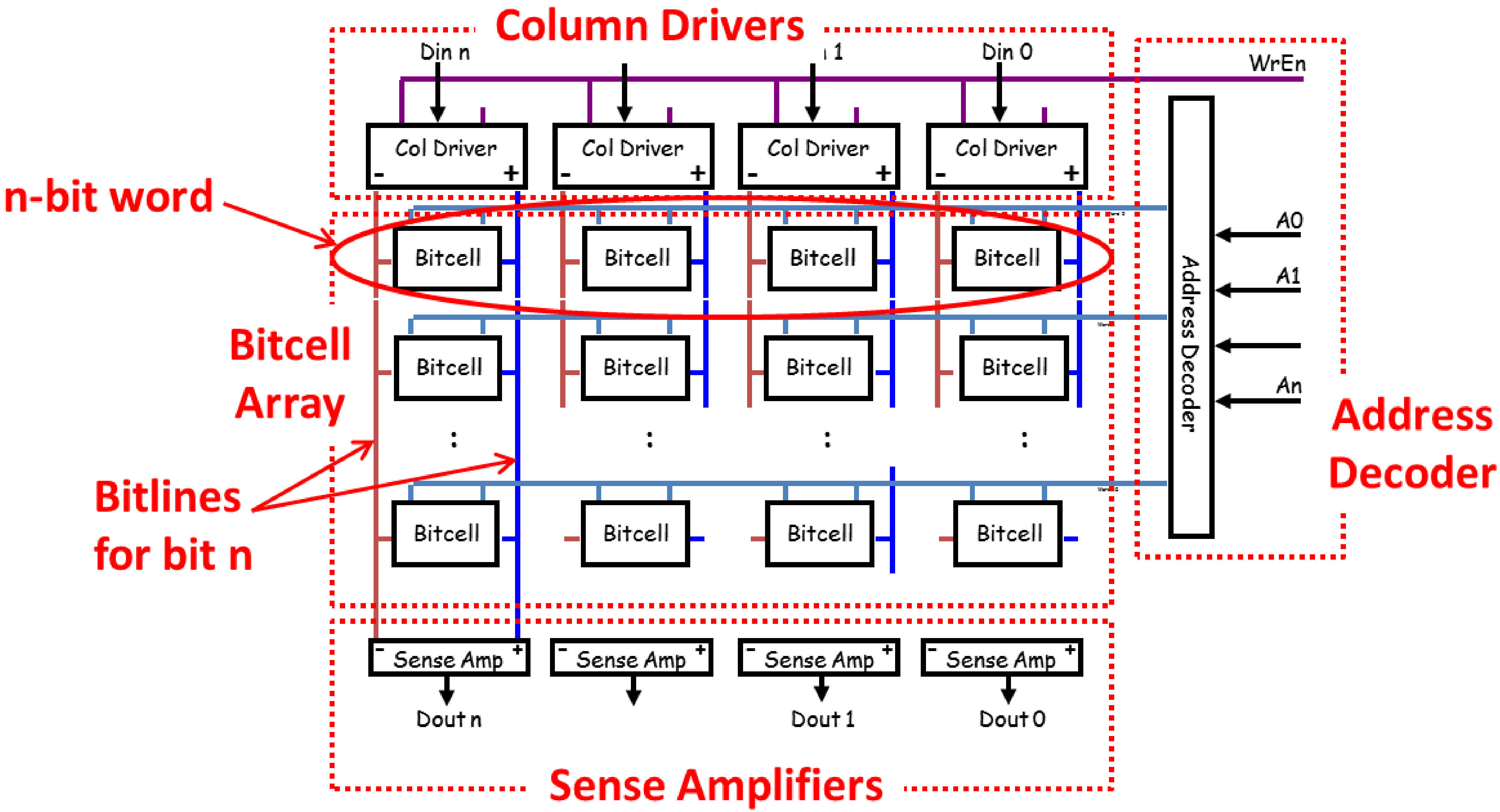
SRAM Operation

- Standby
  - word line de-asserted
- Read
  - precharge bit lines
  - assert WL
  - BL rise/drop slightly
- Write
  - apply value to BL
  - assert WL
  - input drivers stronger



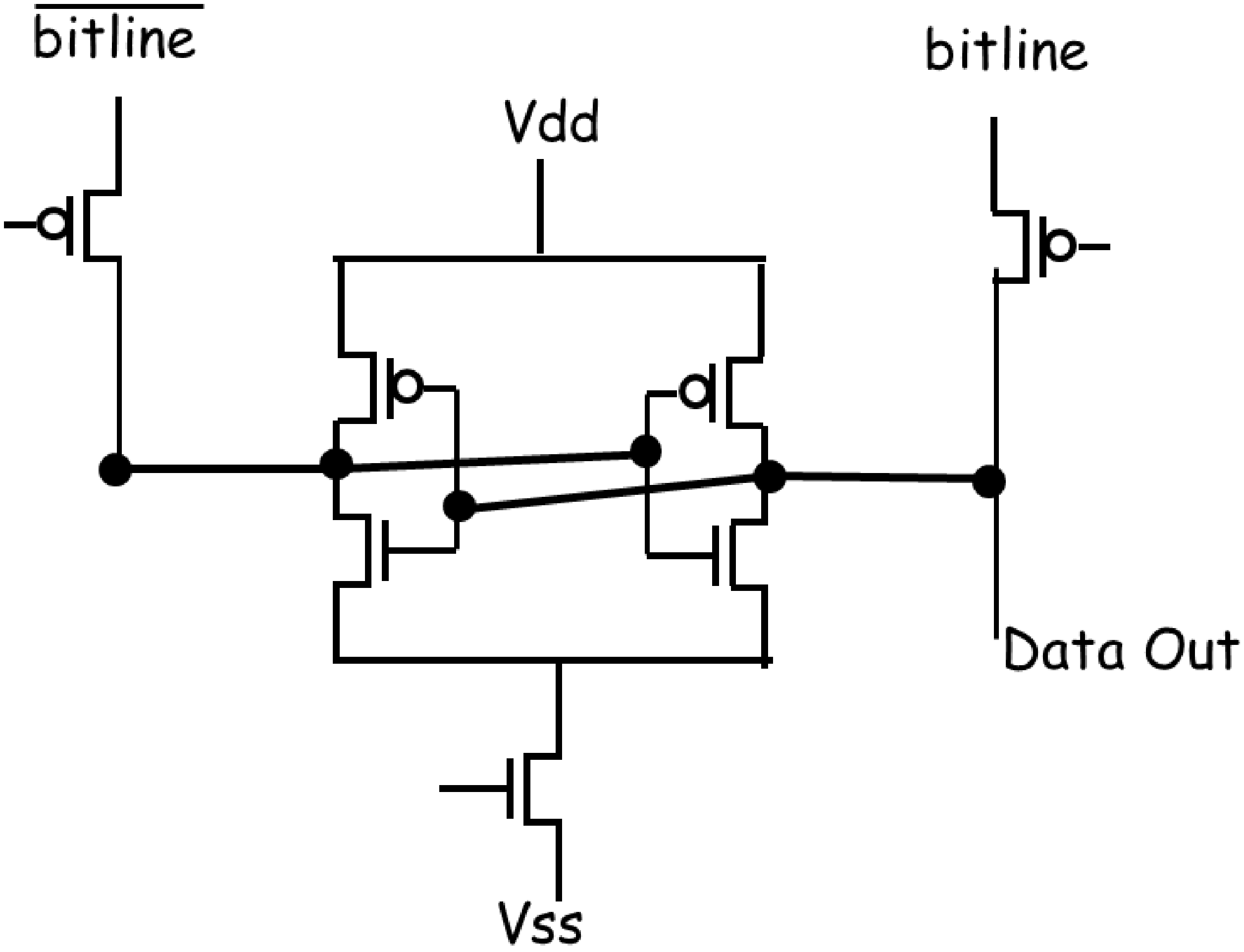


SRAM Architecture

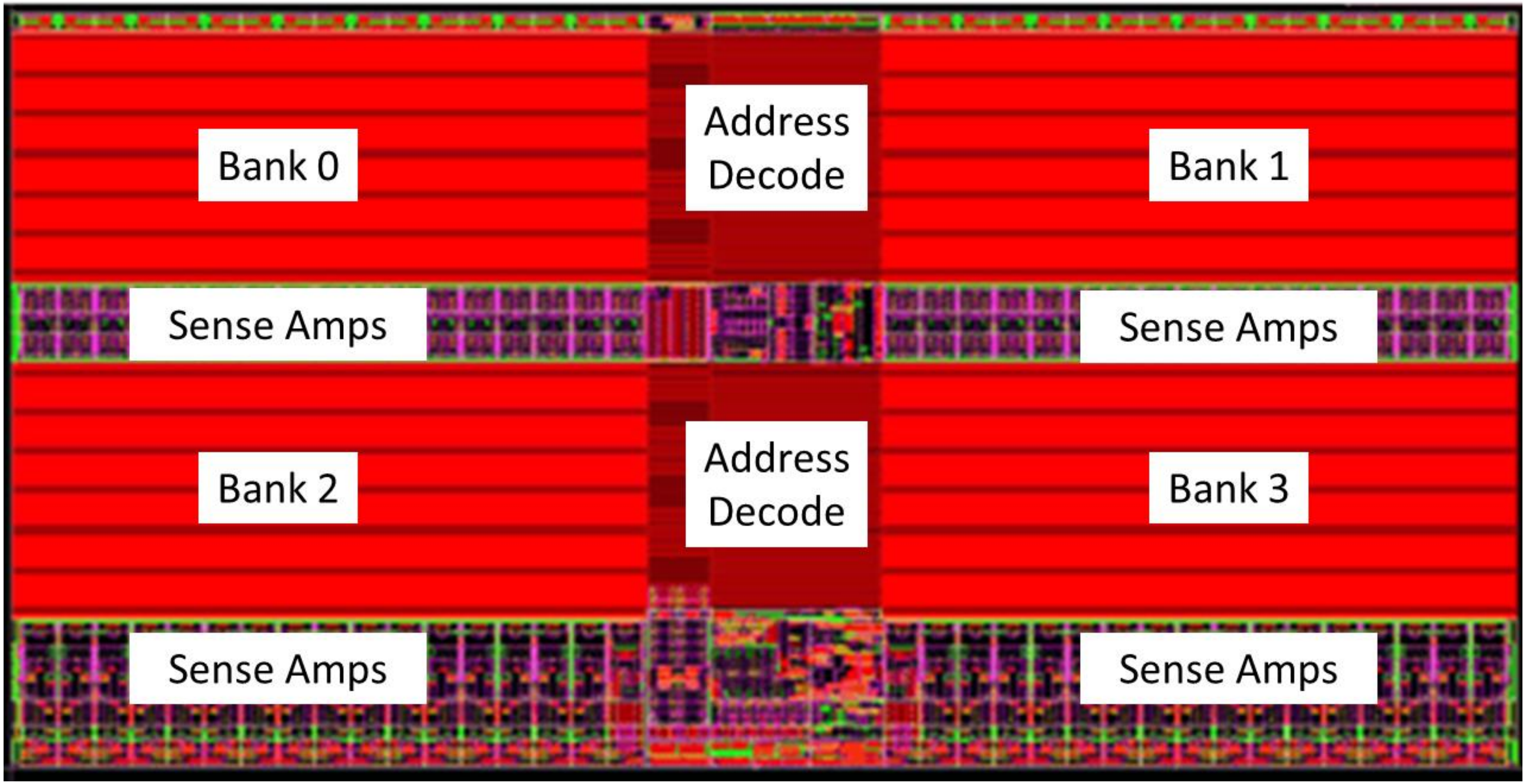


source: semiengineering.com

Sense Amplifier: Differential input



Multi-Bank Layout



source: semiengineering.com

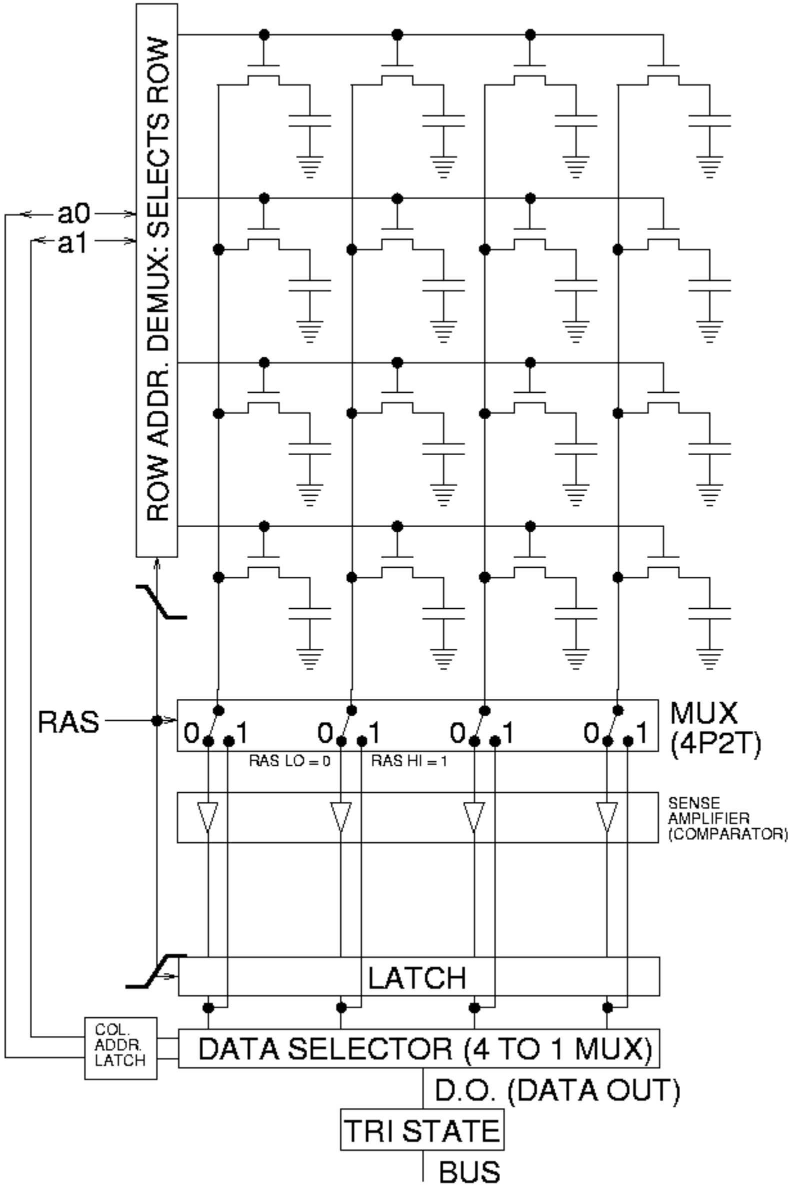
DRAM

- Applications
  - main memory in desktop, laptop, workstation

- Characteristics
  - 1 transistor and 1 capacitor per bit cell
  - need to refresh
  - access time < cycle time
  - slower, less area, cheaper

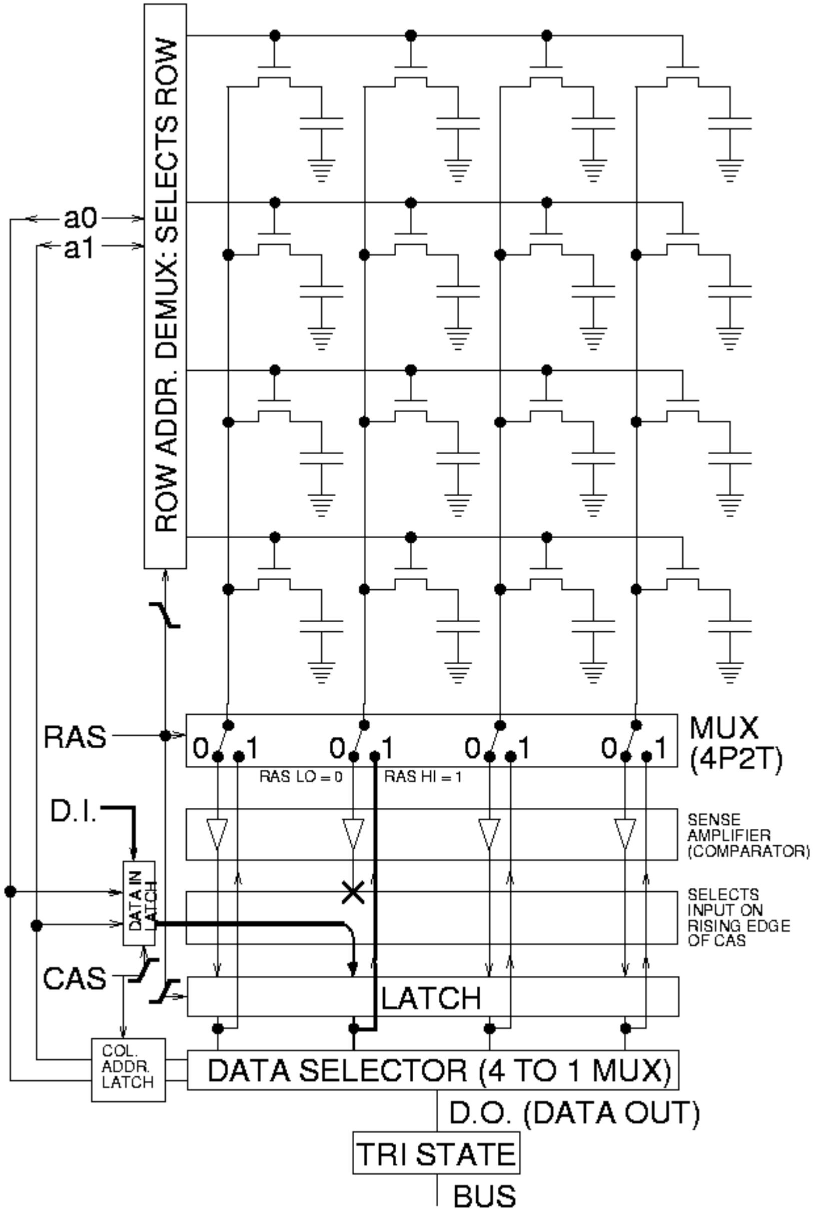
DRAM Read

- disconnect sense amp
- precharge bit lines
- precharge off
- assert wordline
  - transfer charge from cell to bit-line
- detect by sense amp
  - latch output
- read selected column
  - recharge cell
- de-assert word-line



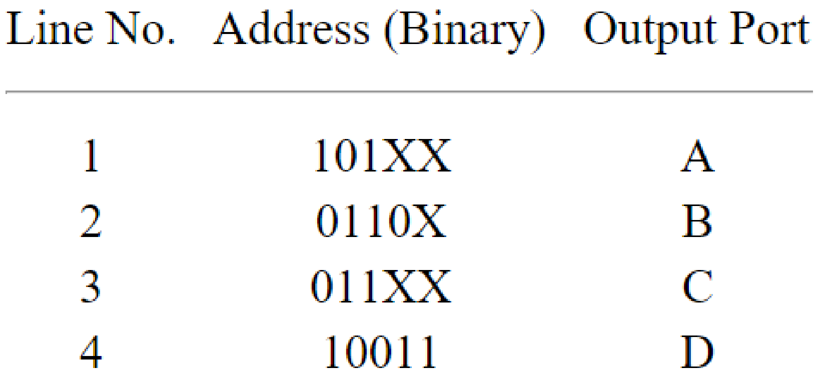
DRAM Write

- select row
- force sense amp to desired value
    - positive feedback
- bit-line to charge cell
- entire row refreshed


ROW ADDR. DEMUX: SELECTS ROW
a0
a1
RAS
0 1
MUX (4P2T)
RAS LO = 0
RAS HI = 1
D.I.
SENSE AMPLIFIER (COMPARATOR)
DATA IN LATCH
SELECTS INPUT ON RISING EDGE OF CAS
CAS
LATCH
COL. ADDR. LATCH
DATA SELECTOR (4 TO 1 MUX)
D.O. (DATA OUT)
TRI STATE
BUS

Content-Addressable Memory (CAM)

- Associative memory
  - used in high-speed searching application
  - e.g. networking routers



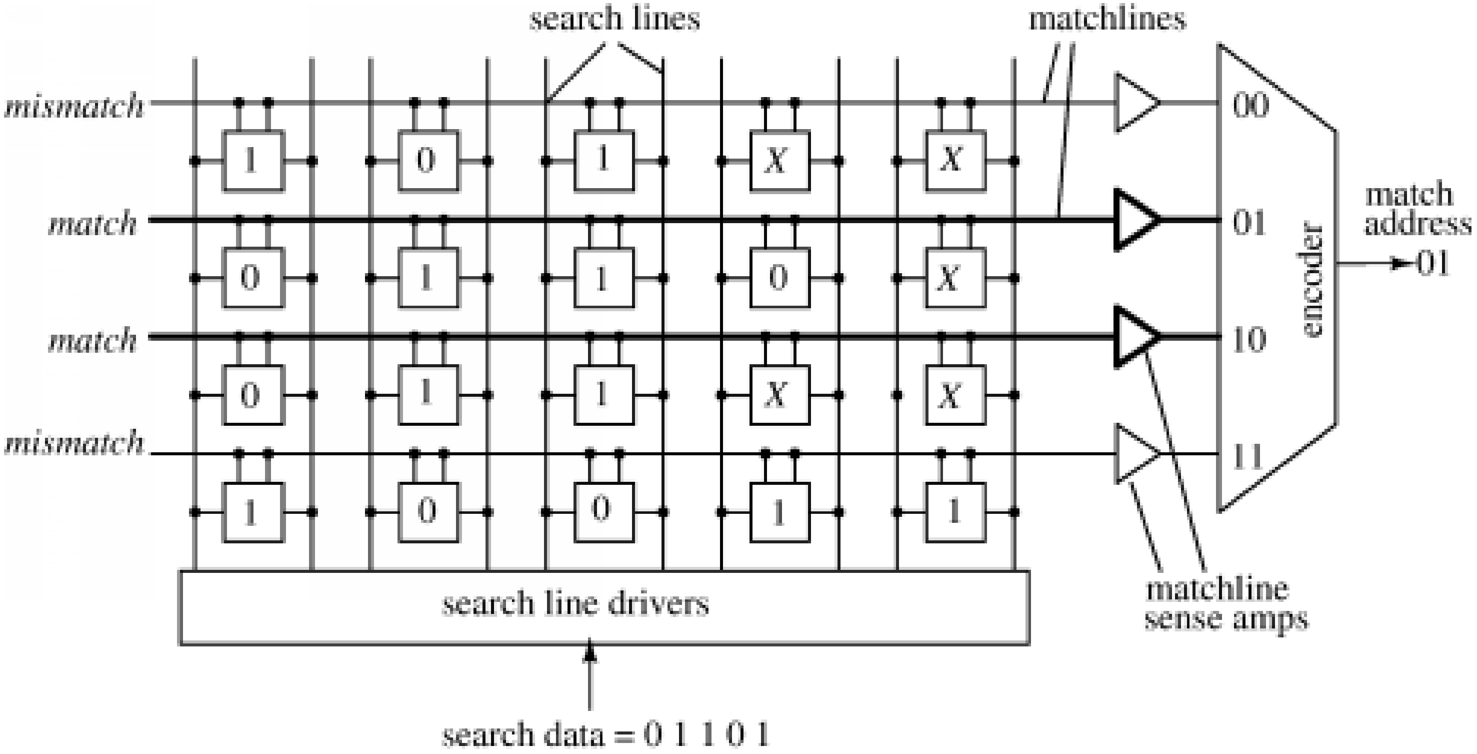
Line No.	Address (Binary)	Output Port
1	101XX	A
2	0110X	B
3	011XX	C
4	10011	D

Simplified routing table

  - more power, area, circuitry

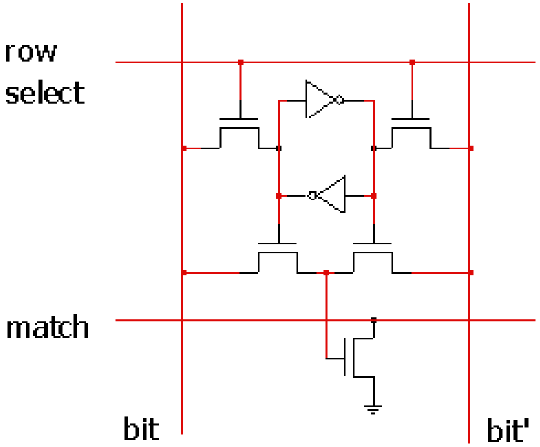
CAM Operation

- NOR-based CAM architecture
  - precharge matchlines
  - broadcast search data
  - CAM cell compare, matchline pulled down if mismatch
  - generate search address/location

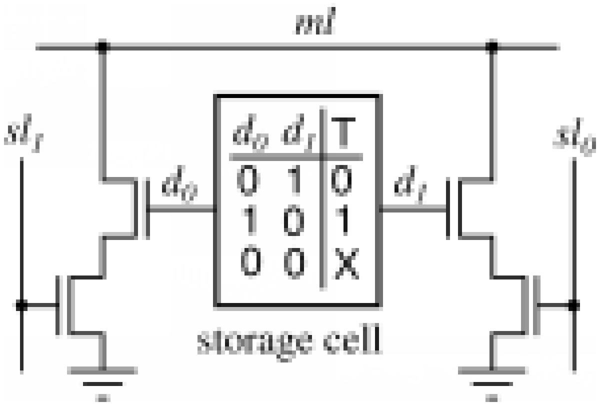


CAM Circuit

- CAM cell

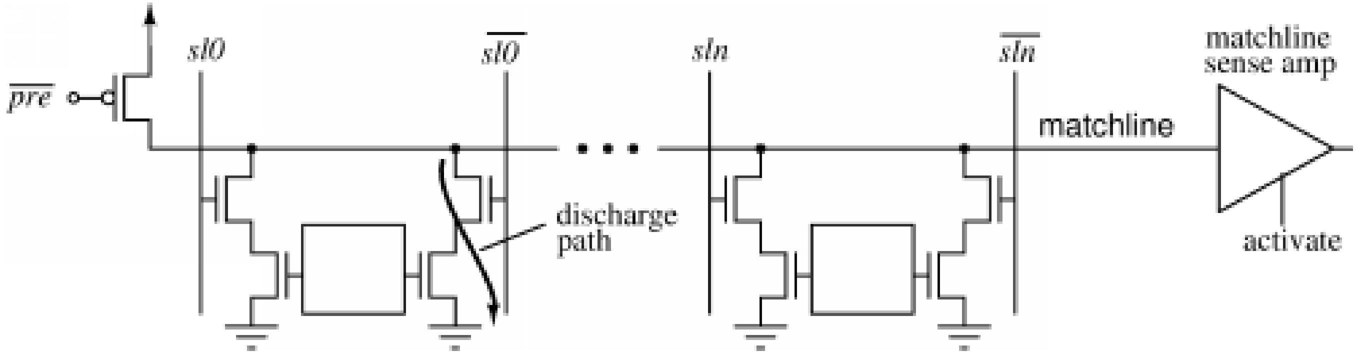


Binary CAM Cell



d_0	d_1	T
0	1	0
1	0	1
0	0	X

Ternary CAM Cell



source: pagiamtzis.com/cam/camintro

Summary

Number Representation

Boolean Logic and Gates

Combinational Logic

Arithmetic Logic

Sequential Logic

Memory Circuit

Review Quiz

- 50 minutes
- Closed Book. No references
- No electronic devices (including calculator)

Outline

More Reviews

Linux Basics

VCS Simulator

Linux Lab

- https://linuxlab.seas.wustl.edu/equeue/
- Remote Linux Desktop
  - virtual network computing (VNC)
  - eQUEUE
  - Javascript, Jave Runtime Environment (JRE)

Linux Basics

- GUI
  - file management
  - folder navigation
- Terminal
  - command-line interface

- Introduction to Linux
  - https://www.edx.org/course/introduction-linux-linuxfoundationx-lfs101x-0

Useful Commands

- Navigation
  - ls, cd, pwd, ln, find, less, more
- Manipulation
  - cat, cp, mv, grep, mkdir, touch
  - chmod, chown
- Check status
  - df, du, quota, uname, history
- Set Environment
  - Unix shell: Bash, C shell (csh, tcsh), etc.
  - source .bashrc
  - module avail

Questions?

Comments?

Discussion?