

ESE 461 Design Automation for Integrated Circuit Systems

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http://classes.engineering.wustl.edu/ese461/

You are in the wrong class if you

- Have never taken a digital logic class (like CSE 260) before;
- Have never heard of MOSFET or CMOS or transistors before;
- Think writing and debugging programs are excruciatingly painful;
- Don't like reasoning about automation algorithms for repetitive tasks;
- Are not interested in designing your very own integrated circuit chips.



Course Objectives



- Understand the design flow of modern IC
 - Very-large-scale integration (VLSI)
 - language: Verilog
 - tools: Synopsys, Cadence
 - process: design, simulation, synthesis, verification, test
 - principles: performance, power, other considerations
- Understand the basics of design automation
 - study the basic algorithms used in VLSI design
 - learn the automation techniques used in the tools
- Pique your interest to learn more on your own
 - introduce some cutting-edge research topics

Tentative Syllabus

- W1: Intro. Review combinational logic.
- W2: Labor day. Review sequential logic.
- W3: Review quiz, Linux and VCS tutorial.
- W3-W4: Verilog. Intro of design flow.
- W5: Logic synthesis.
- W6: Timing analysis.
- W7: Physical design.
- W8: Fall break. Class project intro.
- W9: I/O design and RC extraction.
- W10: Power optimization.
- W11: Hardware acceleration. HLS.
- W12: Reliability and security.
- W13: Conclusion. Thanksgiving.
- W14: Project presentation.





What is the big deal about IC?



Moore's Law





Photo Credit: Intel

Inside an iPad Air 2





iPad Main Board





Interface to the Physical World: The camera





Digital Logic (Interface, Timing, Processing, Output)

Apple iPhone: The quintessential smart system





- Apple A8 APL1011 SoC + SK Hynix RAM as denoted by the markings H9CKNNN8KTMRWR-NTH (we presume it is 1 GB LPDDR3 RAM, the same as in the iPhone 6 Plus)
- Qualcomm MDM9625M LTE Modem
- Skyworks 77802-23 Low Band LTE PAD
- Avago A8020 High Band PAD
- Avago A8010 Ultra High Band PA + FBARs
- SkyWorks 77803-20 Mid Band LTE PAD
- InvenSense MP67B 6-axis Gyroscope and Accelerometer Combo



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CPU

GPU



Why should we care now?

Bell's Law of Computer Classes: A new computing class roughly every decade





"Roughly every decade a new, lower priced computer class forms based on a new programming platform, network, and interface resulting in new usage and the establishment of a new industry." - Adapted from D. Culler



DMEM

IMEM



Intel[®] 4004 processor Introduced 1971 Initial clock speed

108 KHz Number of transistors

2,300 Manufacturing technology

10µ

source: Intel, U. Michigan

15x size decrease 40x transistors 55x smaller λ

emperature ... Timer Sensor Power gated Partially gated Not gated **UMich Phoenix Processor** Introduced 2008 Initial clock speed 106 kHz @ 0.5V Vdd Number of transistors 92,499 Manufacturing technology 0.18 µ

52x40 DMEM

Power

Management

CPU

Clock Gen, PMU

IROM

ompres CPU

I/O

64x10 IMEM

128x10 IROM

Clock Generator

System Bus



Quad-Core Intel[®] Xeon[®] processor Quad-Core Intel® Core™2 Extreme processor Introduced 2006 Intel[®] Core[™]2 Quad processors Introduced 2007 Initial clock speed

2.66 GHz Number of transistors 582,000,000 Manufacturing technology

65nm

Case Study: Internet-of-Things (IoT)



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Case Study: Internet-of-Things (IoT)



Libelium Smart World



Smart Roads

Warning messages and diversions

Case Study: Deep Learning Hardware

- Artificial Intelligence (AI)
- Machine Learning
 - a branch of machine learning
 - deep neural networks (DNN)
 - convolutional neural networks (CNN)
 - recurrent neural networks (RNN)



Artificial intelligence now fits inside a USB stick

) Everywhere you go, you'll always take the neural network with you)

Aaron Souppouris , @AaronIsSocial 04.28.16 in Robots

Com

655 Shares





Case Study: Deep Learning Hardware





Nervana Engine delivers deep learning at ludicrous speed!

Nervana is currently developing the Nervana Engine, an application specific integrated circuit (ASIC) that is custom-designed and optimized for deep learning.

Training a deep neural network involves many compute-intensive operations, including matrix multiplication of tensors and convolution. Graphics processing units (GPUs) are more well-suited to these operations than CPUs since GPUs were originally designed for video games in which the movement of on-screen objects is governed by

Discoverin



vectors and linear algebra. As a result, GPUs have become the go-to computing platform for deep learning. But there is much room for improvement — because the numeric precision, control logic, caches, and other architectural elements of GPUs were optimized for video games, not deep learning.

Case Study: Deep Learning Hardware

- Study group planned
 - meet once a week (Sunday afternoon)
 - faculty-moderated, students-led
 - read classic foundational papers in depth
 - discuss and criticize current research
 - envision emerging technology direction
- Objective
 - participate and lead the change
 - cultivate the habit of research
 - curate a community with shared interest, understanding and language, but diverse ideas





Course Objectives

Motivations

Course Administrivia

Instructional Staff (see homepage for contact info, office hours)



Xuan 'Silvia' Zhang (Tue 4-5pm)

Dengxue Yan (Thur 3:30-5pm)



Prerequisites



- ESE 232: Introduction to Electronic Circuits
 - analysis and design of transistors
 - semiconductor memory devices
- ESE 260: Introduction to Digital Logic and Computer Design
 - combinational and sequential logic
 - logic minimization, propagation delays, timing
- Plus but not required
 - basic computer architecture
 - basic hardware description language (Verilog, VHDL)
 - basic Linux commands

Course Overview



- Course homepage:
 - http://classes.engineering.wustl.edu/ese461/
- Distribution
 - 30%: reading and learning
 - 70%: programming, debugging, design iteration
- Workload
 - no mid or final exams
 - in-class review quiz
 - homework
 - labs
 - one group final project
- Philosophy
 - learner-directed instruction

Final Project



- Goal: <u>learn by doing</u>
 - Work in teams of 2
 - Choose from a few suggested projects
 - Release around Week 8
 - Optimize design to meet/exceed performance goals
 - A custom designed IC chip as the end result
- Evaluation
 - Completion of the design flow
 - Performance achieved
 - Techniques applied
 - Presentation
 - Report

Grading



- Engagement 5%
- Review Quiz 10%
- Homework 10%
- Labs 40%
- Final Project 35%
- Policy:
 - 90% or above A
 - 80% 89% B
 - 65% 79% C
 - 45% 64% D
 - 44% or below F

Policies



- Submission
 - quiz, labs, homework due in class
 - 2-day grace period, then 50% penalty
 - no credits after 1 week, no exception
- Discussion & Collaboration
 - learning through discussion
 - help classmates to understand concepts
 - sharing code or schematics not-allowed
- Plagiarism
 - zero tolerance
 - specify sources to avoid confusion

Textbook



- Lecture Slides and Notes
- Tutorials
- Documentations
- Recommended Textbook
 - Application-Specific Integrated Circuits (ASICs... the book), by Michael John Sebastian Smith
 - online at EDACafe
 - http://www10.edacafe.com/book/ASIC/ASICs.php

Make and Hack





• Explore and Have Fun



Questions?

Comments?

Discussion?