



Lecture 18

Design For Test (DFT)

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- Two Stages
 - Wafer test, one die at a time, using probe card
 - production tester applies signals generated by a test program (test vectors) and measures the ASIC test response.
 - either the customer, or the ASIC manufacture, or both, develops the test program
 - Final test, after packaging, board level
- Failure Analysis
 - Determine the failure mechanism
 - Due to the soldering process, electrostatic damage during handling, or others between shipping and testing
 - If the problem is from ASIC fabrication, the test program may be inadequate
 - Board level failure field repair are expensive

Importance of Test



- Defect level is used to measure product quality
 - 10 defective chips in 100,000 => defect level is 0.1 percent or 100ppm
 - Average quality level (AQL) = 1 - defect level

TABLE 14.1 Defect levels in printed-circuit boards (PCB). ¹

ASIC defect level	Defective ASICs	Total PCB repair cost
5%	5000	\$1million
1%	1000	\$200,000
0.1%	100	\$20,000
0.01%	10	\$2,000

TABLE 14.2 Defect levels in systems. ²

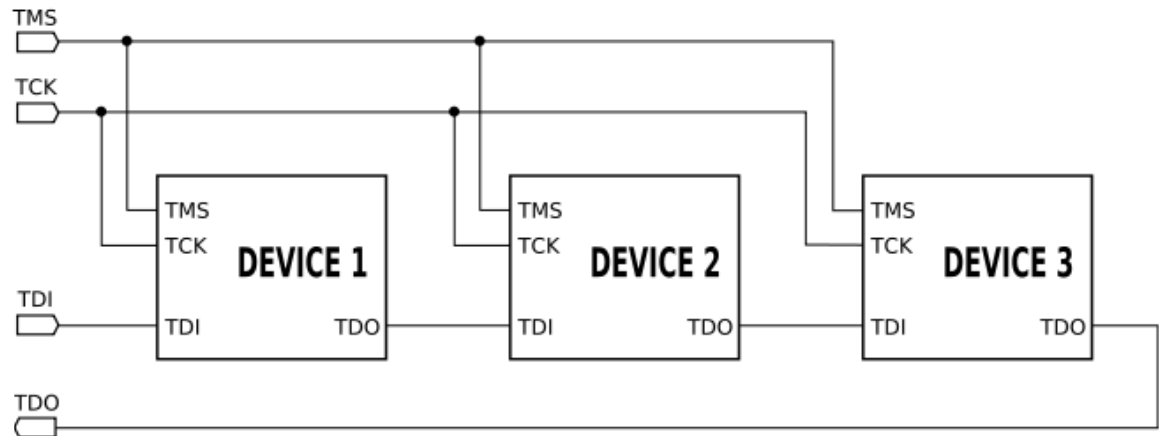
ASIC defect level	Defective ASICs	Defective boards	Total repair cost at system level
5%	5000	500	\$5 million
1%	1000	100	\$1 million
0.1%	100	10	\$100,000
0.01%	10	1	\$10,000

Boundary Scan Test



- Joint Test Action Group (JTAG) 2.0, or IEEE Standard 1149.1
 - boundary - Scan Test (BST) standard, using a 4/5-wire interface
 - for PCB and packaging testing
- Add a special logic cell to each ASIC I/O pad
 - these cells are joined together to form a chain and create a boundary-scan shift register

1. **TDI** (Test Data In)
2. **TDO** (Test Data Out)
3. **TCK** (Test Clock)
4. **TMS** (Test Mode Select)
5. **TRST** (Test Reset) optional.



- Fabrication of ASIC may introduce a defect that in turn may cause a fault.
- Two common type of defects in metallization
 - Underetching the metal : bridge or short circuit
 - Overetching the metal: break or open circuits
- Other defects
 - Dicing, mounting, wafer probing, wire bonding
 - Electrical, thermal, corrosion, stress, adhesion failure, cracking, contaminated chemicals, dirty environment

- Infant Mortality
 - if defects are nonfatal but to cause failures early in the life of a product.
- Bathtub Curve
 - failure rates decrease rapidly to a low value that remains steady until the end of life when failure rates increase again.
- Wearout Mechanism
 - hot-electron wearout, electromigration, etc.

- Burn-in Test
 - catch susceptible early failure
 - operating an ASIC in an elevated temperature accelerates this type of failure, or apply additional stresses, such as elevated current or voltage
- Metrics
 - mean time between failures (MTBF) for a repairable produce
 - mean time to failure (MTTF) for a fatal failure
 - failure in time (FITs) when 1 fit equals a single failure in 10^9 hours
 - sum the FITs for all the components in a product to determine an overall measure for the product reliability
 - Microprocessor (standard part) 5 FITs
 - 100 TTL parts, 50 parts at 10 FITs, 50 parts at 15 FITs
 - 100 RAM chips, 6 FITs

The overall failure rate for this system is $5 + 50 \times 10 + 50 \times 15 + 100 \times 6 = 1855$ FITs.

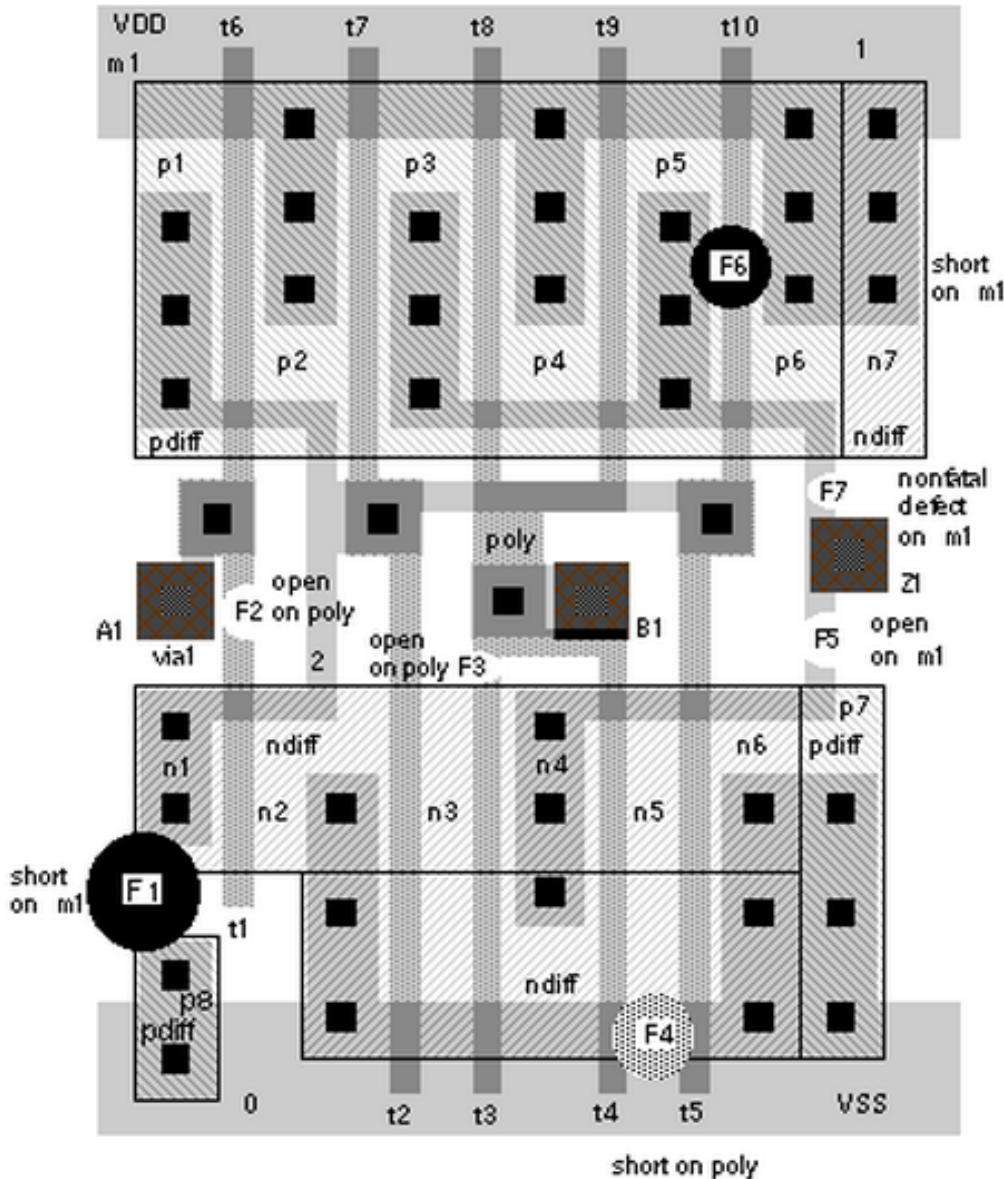
- Open-Circuit Fault
 - bad contact
- Short-Circuit Fault
 - accidentally connected
 - also called bridging faults
- Degradation Fault
 - parametric fault: incorrect switching threshold
 - delay fault: a critical path being slower than specification
- Physical Fault vs. Logical Fault

Fault Models



Fault level	Physical fault	Degradation fault	Logical fault	
			Open-circuit fault	Short-circuit fault
Chip	Leakage or short between package leads	.		.
	Broken, misaligned, or poor wire bonding		.	
	Surface contamination, moisture	.		
	Metal migration, stress, peeling		.	.
	Metallization (open or short)		.	.
Gate	Contact opens		.	
	Gate to S/D junction short	.		.
	Field-oxide parasitic device	.		.
	Gate-oxide imperfection, spiking	.		.
	Mask misalignment	.		.

Physical Faults



F1 is a short between m1 lines and connects node n1 to VSS.

F2 is an open on the poly layer and disconnects the gate of transistor t1 from the rest of the circuit.

F3 is an open on the poly layer and disconnects the gate of transistor t3 from the rest of the circuit.

F4 is a short on the poly layer and connects the gate of transistor t4 to the gate of transistor t5.

F5 is an open on m1 and disconnects node n4 from the output Z1.

F6 is a short on m1 and connects nodes p5 and p6.

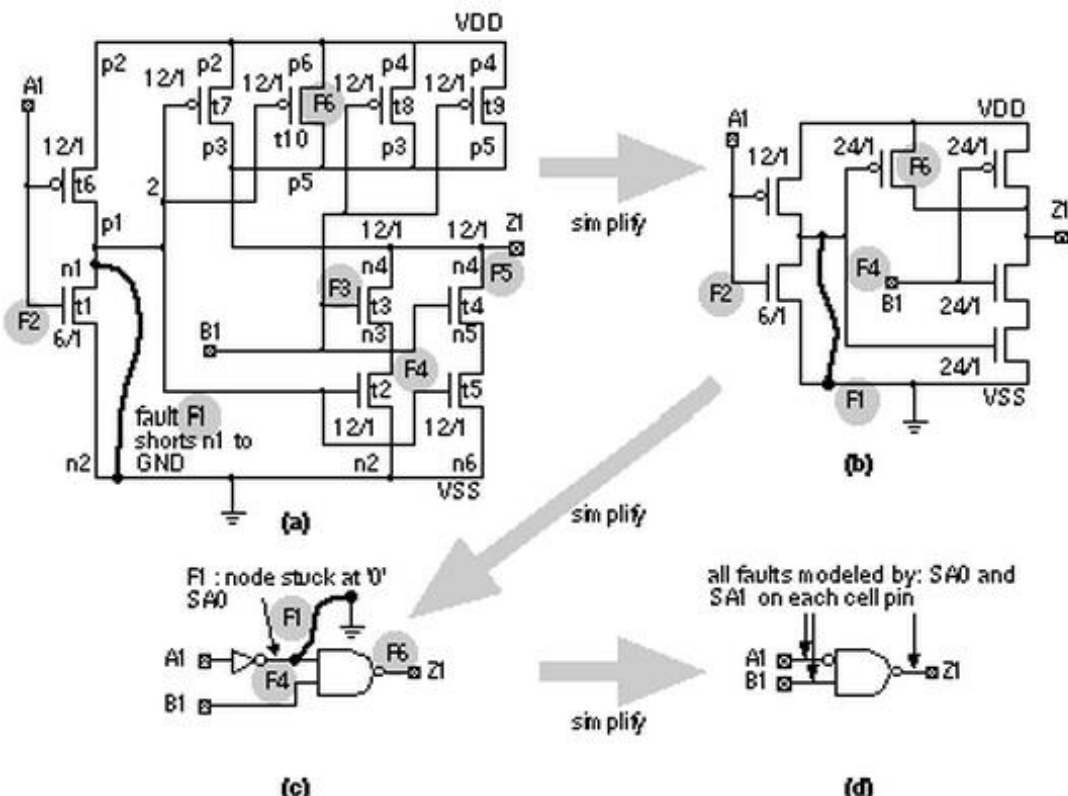
F7 is a nonfatal defect that causes necking on m1.

Logical Faults



Stuck-at Fault model

1. Stuck at 1 fault (SA1 or s@1)
2. Stuck at 0 fault (SA0 or s@0)



F1 translates to node n1 being stuck at 0, equivalent to A1 being stuck at 1.

F2 result in node n1 remaining high, equivalent to A1 being stuck at 0.

F3 will affect half of the n -channel pull-down stack and may result in a degradation fault. The cell will still work, but the fall time at the output will double. A fault such as this is extremely hard to detect.

F4 is a bridging fault whose effect depends on the relative strength of the transistors driving this node.

F5 completely disables half of the n -channel pulldown stack and will result in a degradation fault.

F6 shorts the output node to VDD and is equivalent to Z1 stuck at 1.

F7 If this line did break due to electromigration the cell could no longer pull Z1 up to VDD. This would translate to a Z1 stuck at 0. This fault would probably be fatal and stop the ASIC working.

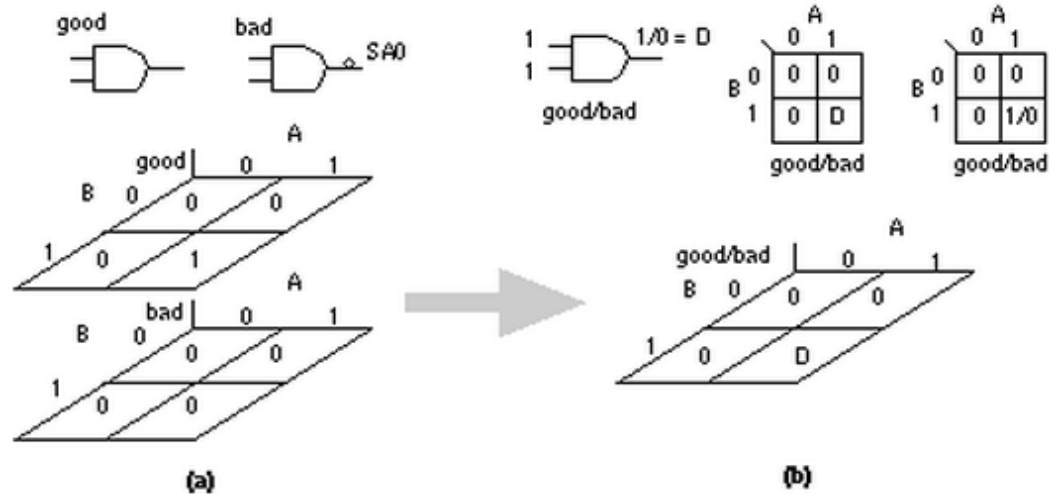
- Stuck-at-0
 - represent a signal that is permanently low regardless of the other signals that normally control the node
- Stuck-at-1
 - represent a signal that is permanently high regardless of the other signals that normally control the node
- Example
 - assume that you have a two-input AND gate that has a stuck-at-0 fault on the output pin
 - regardless of the logic level of the two inputs, the output is always 0

- Preconditions for Detecting
 - the node of a stuck-at fault must be controllable and observable for the fault to be detected
- Controllable Node
 - if you can drive it to a specified logic value by setting the primary inputs to specific values
 - a primary input is an input that can be directly controlled in the test environment
- Observable Node
 - if you can predict the response on it and propagate the fault effect to the primary outputs where you can measure the response
 - a primary output is an output that can be directly observed in the test environment

Automatic Test-Pattern Generation



- D(etect)-Calculus
- Enabling Value
 - propagate a signal
- Controlling Value
 - opposite of enabling value
 - fix the output



AND	0	1	D	0	1	X
0	0	0	0	0	0	0
1	0	1	0	0	1	X
D	0	D	0	0	D	X
D	0	D	0	0	D	X
X	0	X	X	X	X	X

OR	0	1	D	0	1	X
0	0	1	D	0	1	X
1	1	1	1	1	1	1
D	D	1	D	1	D	X
D	D	1	D	1	D	X
X	X	1	X	X	X	X

NAND	0	1	D	0	1	X
0	1	1	1	1	1	1
1	1	0	1	0	X	X
D	1	D	1	1	X	X
D	1	D	1	0	X	X
X	1	X	X	X	X	X

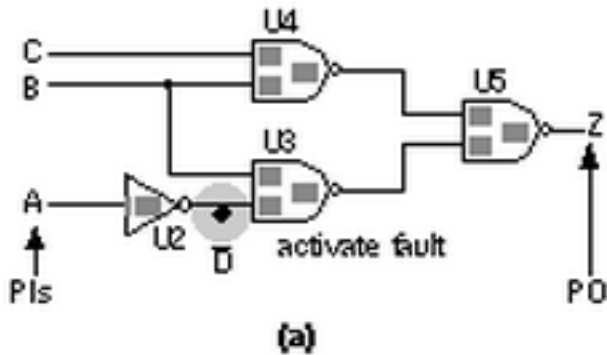
NOR	0	1	D	0	1	X
0	1	0	D	0	X	X
1	0	0	0	0	0	0
D	D	0	D	0	X	X
D	D	0	D	0	X	X
X	X	0	X	X	X	X

Automatic Test-Pattern Generation

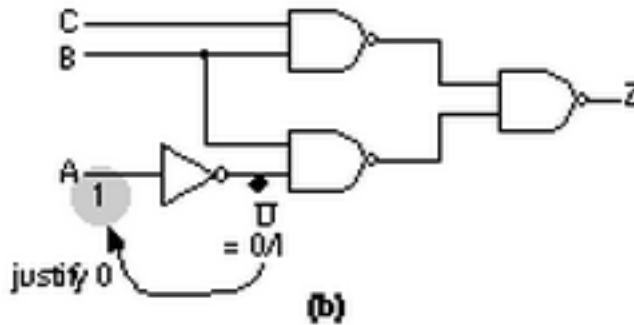


- Find an input vector to test a fault origin
- Work backward until reach a PI (primary input)
- Work forward using sensitized path to a PO
 - a wave of D's is called the D-frontier

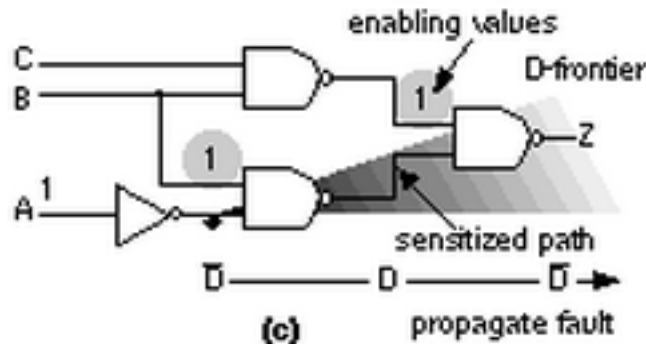
1. Choose a fault



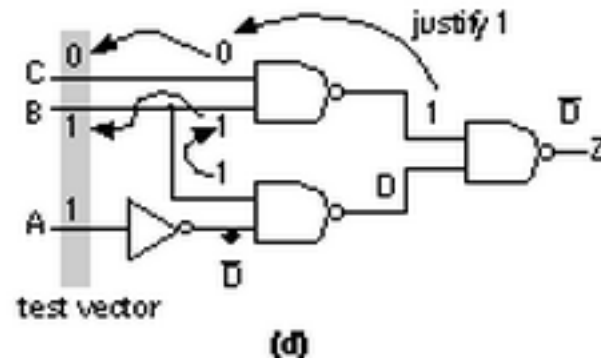
2. Work backward



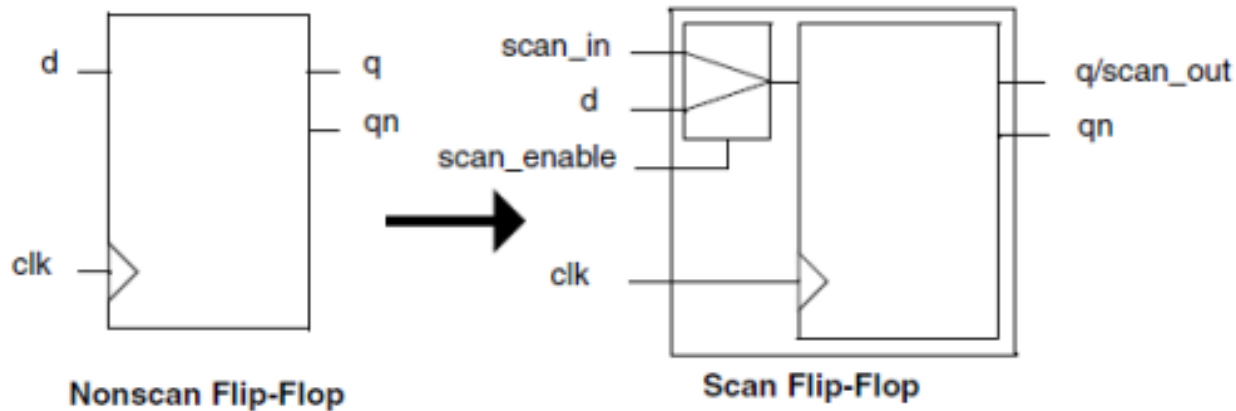
3. (N)AND gates to 1, (N)OR gates to 0



4. Work backward



- Insert scan chain in netlist
 - replacing flip-flops with multiplexed flip-flops

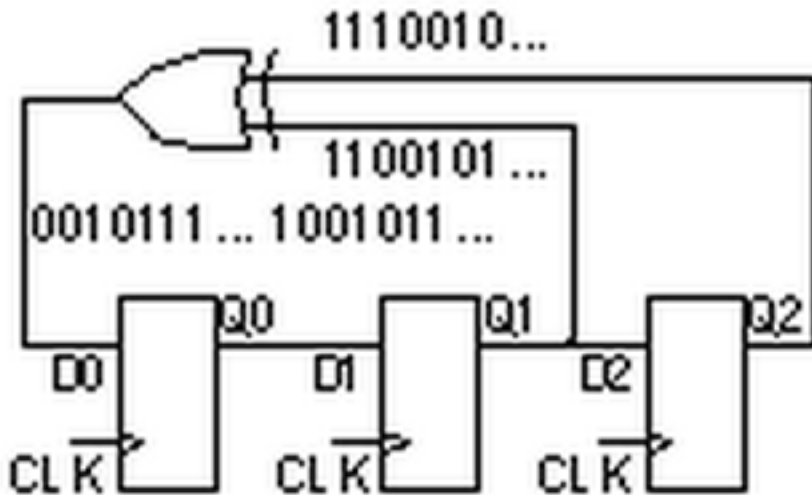


- Increase observability/controllability of non-sequential logic throughout the chip

Built-in Self-Test (BIST)



- LFSR (Linear feedback shift register)
 - Based on primitive polynomials
- PRBS (pseudorandom binary sequence)



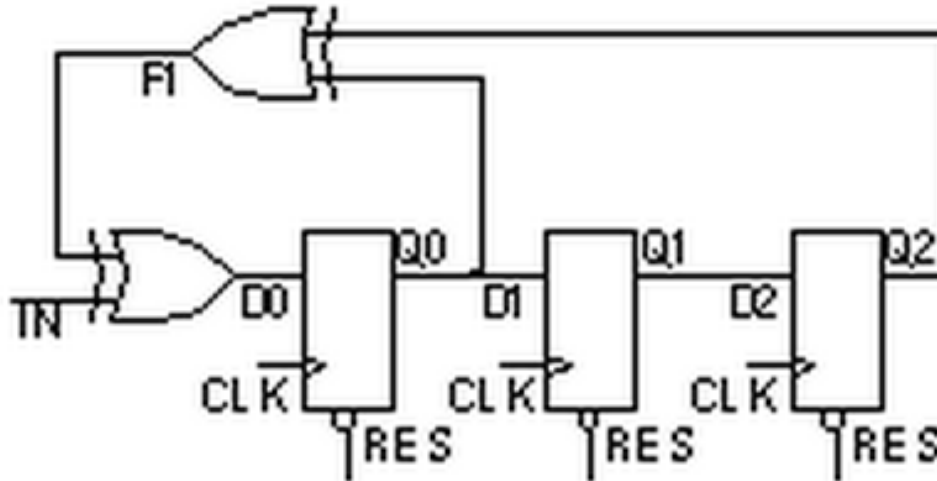
Clock tick, t =	$Q0_{t+1} = Q1_t \oplus Q2_t$	$Q1_{t+1} = Q0_t$	$Q2_{t+1} = Q1_t$	Q0Q1Q2
1	1	1	1	7
2	0	1	1	3
3	0	0	1	1
4	1	0	0	4
5	0	1	0	2
6	1	0	1	5
7	1	1	0	6
8	1	1	1	7

- Initial state is not all zeros
- Maximal length sequence

Built-in Self-Test (BIST)

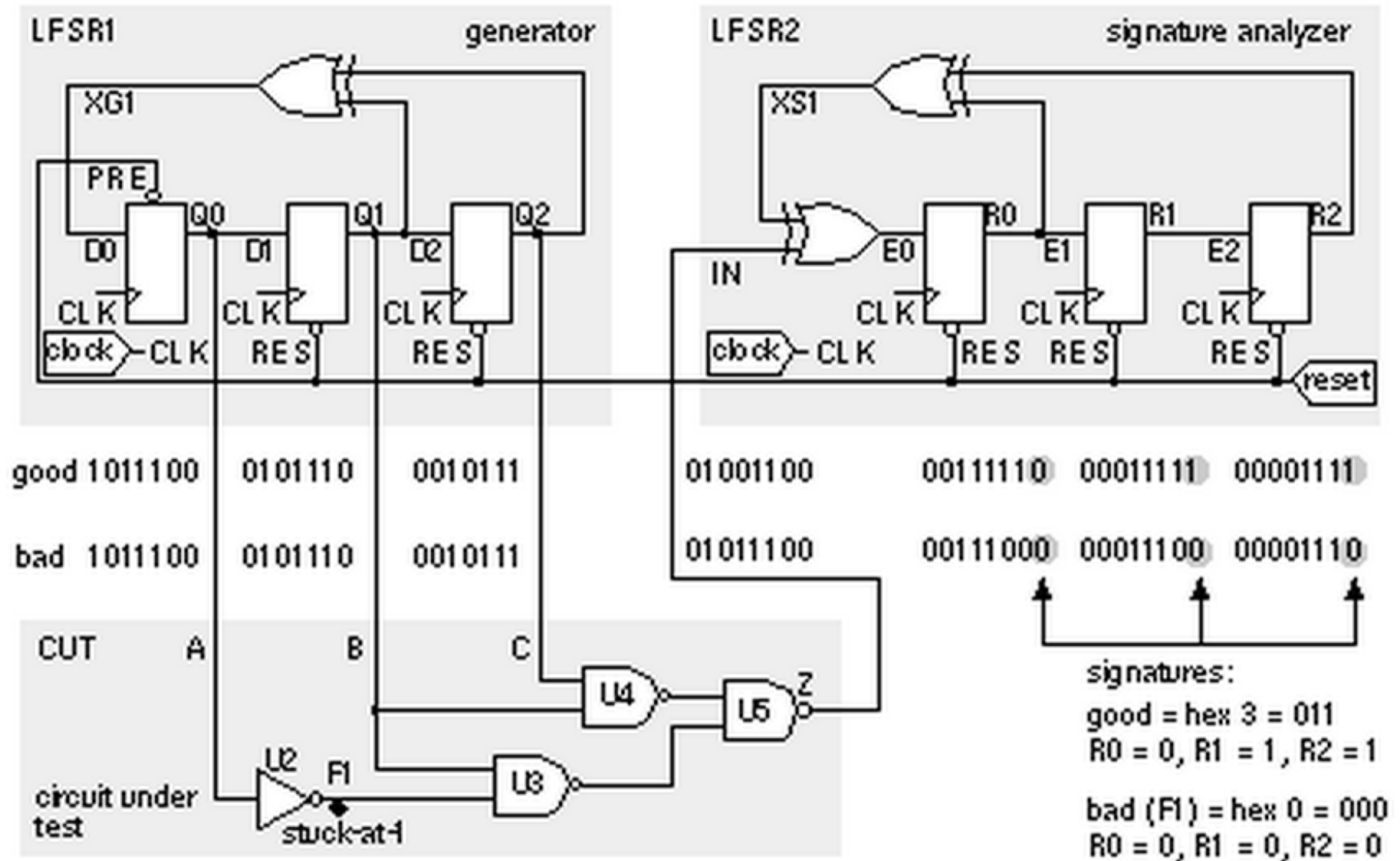


- Serial input signature register (SISR)
- Data compaction (compression)
- Signature (at the end of input sequence) analysis



- If input sequence and SISR are long enough, it is unlikely (though possible) that two different input sequences will produce the same signature

Built-in Self-Test (BIST)



Reference



- ASIC ebook, Chapter 14



Questions?

Comments?

Discussion?