ESE 461: Design Automation for Integrated Circuit Systems

Lab 4

Due: Oct 19, 2:30 pm

Submission Instructions:

1. Summit all your source Verilog codes (i.e. all the .v files). The code must be clear, organized and readable with comments.

2. Submit the screen snapshot showing the *vcs* command used to compile the simulation and the output messages showing successful compilation. (Use Alt-Print-screen to capture a window to clipboard and then paste to word).

3. Submit the screen snapshot of graphical simulation waveforms in *dve*. (Use Alt-Print-screen to capture a window to clipboard and then paste to word).

4. (Optional) Write a short report to summarize your results, debugging process and anything else you think may help us understand your code and result.

Put all files in one folder named: *lab4_First name_Last name_Student ID_fall_2016_ese461.* Then compress it into a .zip file using:

zip -r lab4_First name_Last name_Student ID_fall_2016_ese461.zip lab3_First name_Last name_Student ID_fall_2016_ese461

and send the zip file to TA's email: dengxue.yan@wustl.edu

For example:

First name is : Bob

Last name is : Lee

Student ID is: 12345

Then the folder should be *lab4_Bob_Lee_12345_fall_2016_ese461,*

Pack it using:

zip -r *lab4_Bob_Lee_12345_fall_2016_ese461.zip lab4_Bob_Lee_12345_fall_2016_ese461*

Please do not summit files like compiling result(*simv*) or simulation data(*.vpd*).

Lab Question:

Design a dual clock asynchronous 16-bit width FIFO (First In First out) memory with depth of 8:

1. A general memory 8x16 bits must be implemented first, then design control logic so that the FIFO will not overflow.

2. Data read from the FIFO according to the write sequence.

3. If memory is full, then FIFO controller need to deassert *wr_request* to tell the write side to stop write(in the situation when write CLK is greater than Read CLK).

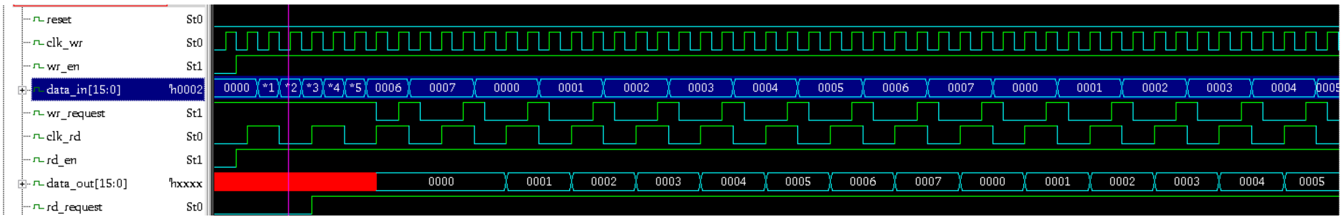
4. If memory is empty, then FIFO controller need to deassert *rd_request* to tell the read side to stop read. (in the situation when Read CLK is greater than Write CLK).

5. *wr_en* is an outside signal used for enable or disable the write process. *rd_en* is an outside signal used for enable or disable the read process.

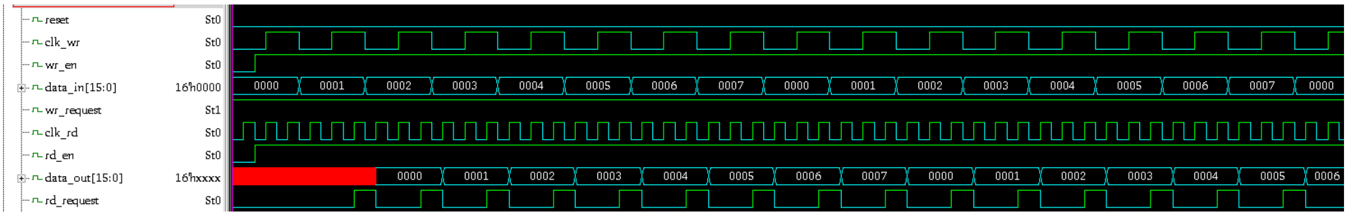
Optional:

Gray code could be used to reduce the probability of errors occurs when the signal and the CLK changes at the same because of the asynchronous Write CLK and Read CLK.

Following figures are 2 examples of the FIFO action.



The Result of Test Bench *FIFO_tb.v* (Write CLK = 3Read CLK)



The Result of Test Bench *FIFO_tb1.v* (3Write CLK = Read CLK)

Reference:

Dual-clock FIFO is often used to interface between two different clock domains. More explanation at

http://www.asic-world.com/tidbits/clock_domain.html

You can also find an example Verilog implementation at http://web.ece.ucdavis.edu/~astill/dcfifo.html

Please use it for reference only. We will check your codes against this example to prevent cheating.