ESE 461: Design Automation for Integrated Circuit Systems

Homework 2

Due: Sep 14, 2:30 pm

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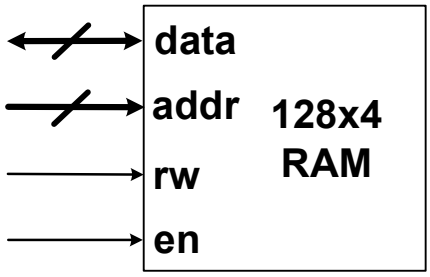
1. 1) Design a 256*4-bit RAM using 128*4-bit modules shown below.

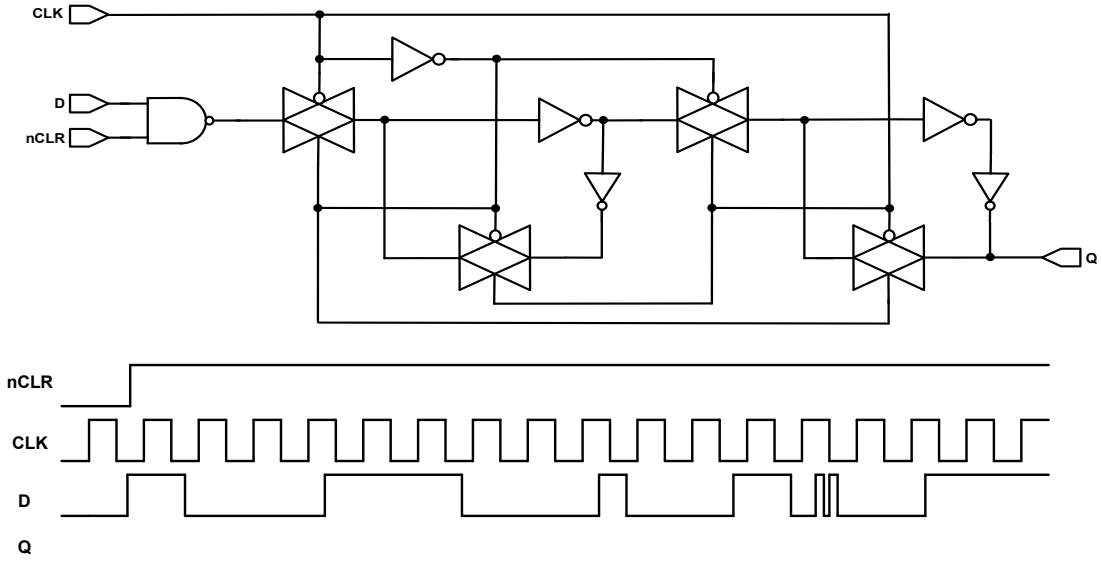
2) Design a 128*8-bit RAM using 128*4-bit modules shown below.



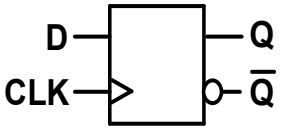
128x4-bit RAM Module

2 A traffic light control at a simple intersection uses a binary counter to produce the following sequence of combinations on lines A, B, C, and D: 0000, 0001, 0011, 0010, 0110, 0111, 0101, 0100, 1100, 1101, 1111, 1110, 1010, 1011, 1001, 1000. After 1000, the sequence repeats, beginning again with 0000, forever. Each combination is present for 5 seconds before the next one appears. These lines drive combinational logic with output to lamps RNS (Red – North/South), YNS (Yellow-North/South), GNS (Green-North/South), REW (Red-East/West), YEW (Yellow-East/West), and GEW(Green-East/West). The lamp controlled by each output is ON for a 1 applied and OFF for a 0 applied. For a given direction, assume that green is on for 30 seconds, yellow is on for 5 seconds, and red is on for 45 seconds. (The red intervals overlap for 5 seconds.) Divide up the 80 seconds available for the cycle through the 16 combinations into 16 intervals and determine which lamps should be lit in each interval based on expected driver behavior. Assume that, for interval 0000, a change has just occurred and that GNS=1, REW=1, and all other outputs are 0. Design the logic to produce the six outputs using AND and OR gates and inverters.

3. The Flip-Flip shown is a master-slave D-FF with clear. The CLK and nCLR is shown below in the timing diagram, and the D input is activated as shown. Plot Q for the number of clock pulses shown (The initial value of Q is 0).



4. Design a 8-bits left-shifter by using D Flip-Flop (the following figure) and AND, OR, NOT gates.



D Flip-Flop

5. Design a finite-state machine that inputs a string of a's and b's (read from left to right) and outputs the number of *a*'s plus twice the number of *b*'s modulo 4, i.e.

$$\boldsymbol{Output} = (\boldsymbol{n_a}+\boldsymbol{2n_b})\%\boldsymbol{4}$$

For instance the input "*abaababbaaaba*" would produce the output "*1301302012312*"

6. Design a finite-state machine for a sequence detector that detects a sequence of 011 on a single input X.

7. Read about the standard of IEEE 754: floating point in modern computers. Then describe how single and double-precision floating-point numbers are represented in a 32-bit computer.