ESE 461: Design Automation for Integrated Circuit Systems

Final Project

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1. Main Objectives

The final project is to review the materials you learned in this class and expose you first hand to the design flow and the commercial design automation tools that are used for the ASIC/VLSI design. Also you will have a chance to implement some real-world algorithms in actual silicon.

2. Requirements

1) Form a team of 3 people and choose one project topic from two options --- *OpticalFlow* and *Bitcoin Hashing*. More detailed description for each topic is provided in Appendix section below.

2) Implement the behavioral-level code of your selected algorithm in Verilog and verify its functionality in VCS simulation.

3) Submit a mid-project report (as a team) including the behavioral Verilog source code, Verilog testbench, and VCS simulation verifying functional correctness.

4) Synthesize your Verilog design using Design Compiler (DC) and place-and-route the synthesized netlist using Encounter.

5) Iterate your design to meet and exceed the required specifications by increasing its speed (operating clock frequency), reducing its power consumption, and minimizing the chip area.

6) Prepare a 15-minute presentation of the project to be delivered in the last week of the class. Each team member has to participate in the presentation.

7) Submit a final report (as a team) detailing your design strategy, process, achieved performance (e.g. clock frequency, total power consumption, and total area) and other related experience (e.g. debugging, optimization, and learning the advanced feature of the tools). You are also expected to submit your Verilog source code and test bench, VCS simulation screen capture, synthesized netlist, physical design screen capture, and GDS file, as well as timing, power, and area reports generated by DC and Encounter. Individual contribution from each team member should be clearly specified in the final report.

3. Project Milestones

No	Date	Event
1	Oct. 28th	Project description released
2	Nov. 23rd	Mid-project report due (30% of total project grade). Late submission by Nov. 28th will be discounted by 40%; late submission after Nov. 28th will not receive any credits.
3	Dec. 8th	Project presentation in class
4	Dec. 12th	Final report is due

4. Submission Instructions

1) Create a folder named "ESE461-Project-MidReport-Team#" or "ESE461-Project-FinalReport-Team#", where # is the team number listed below. Put all submitted files in this folder.

2) Create a README.doc for your submission. In it, list each file you have included in the folder and briefly describe its content.

3) Create an archive (.tar file) following the same instructions as the previous labs. Then Email the archive to TA's email: dengxue.yan@wustl.edu with the subject line the same as the folder/archive name.

Appendix

Project topic options:

Option 1: Optical Flow

1. **Algorithm description (here)**
2. **Sample C code (here)**
3. **Sample C testbench (here)**

Option 2: Bitcoin

1. **Algorithm description (here)**
2. **Sample C code (here)**
3. **Sample C testbench (here)**

Teams:

Team No	*Members*	*Project Topic*
1	Meizhi Wang Longzhen Zhang Alison Gu	Optical Flow
2	Alex Carsello Alex Herriott Ray Xu	Optical Flow
3	Philip Johnston Huy Do Rui Huang	Bitcoin
4	Andrew Ellison Yunfei Gu Xinyao Li	Optical Flow
5	An Zou Weidong Cao Elliot Jaffe	Bitcoin